

# Specification for Approval

**PRODUCT NAME:** RGS15128128WR000  
**PRODUCT NO.:** 9922102000

<b>CUSTOMER</b>
<b>APPROVED BY</b>
<b>DATE:</b>

<b>RITDISPLAY CORP. APPROVED</b>

## REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2008. 07. 10	
X02	<ul style="list-style-type: none"> <li>■ Modify definition of panel thickness</li> <li>■ Add lifetime specifications</li> <li>■ Modify D.C electrical characteristics</li> <li>■ Add panel electrical specifications</li> <li>■ Add application circuit</li> </ul>	2009. 04. 24	Page 5, 6, 7, 8 & 16
A01	<ul style="list-style-type: none"> <li>■ Transfer from X version</li> <li>■ Add the information of module weight</li> <li>■ Modify seal color (white→black)</li> <li>■ Add the packing specification</li> </ul>	2009. 12. 16	Page 5, 18 & 19

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## **1. SCOPE**

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## **2. WARRANTY**

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 128\*128
- Driver IC : SSD1327
- Excellent Quick response time : 10 $\mu$ s
- Extremely thin thickness for best mechanism design : 1.41 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, I<sup>2</sup>C Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

#### 4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 128	dot
2	Dot Size	0.19 (W) x 0.19 (H)	mm <sup>2</sup>
3	Dot Pitch	0.21 (W) x 0.21 (H)	mm <sup>2</sup>
4	Aperture Rate	82	%
5	Active Area	26.86 (W) x 26.86 (H)	mm <sup>2</sup>
6	Panel Size	33.8 (W) x 36.5 (H)	mm <sup>2</sup>
7*	Panel Thickness	1.22 ± 0.1	mm
8	Module Size	33.8 (W) x 43.7 (H) x 1.41 (T)	mm <sup>3</sup>
9	Diagonal A/A size	1.5	inch
10	Module Weight	3.48 ± 10%	gram

\* Panel thickness includes substrate glass, cover glass and UV glue thickness.

## 5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V <sub>ci</sub> )	-0.3	4	V	T <sub>a</sub> = 25°C	IC maximum rating
Supply Voltage (V <sub>cc</sub> )	8	19	V	T <sub>a</sub> = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	10,000	-	Hrs	100 cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Life Time	11,000	-	Hrs	90 cd/m <sup>2</sup> , 50% checkerboard	Note (2)
Life Time	12,000	-	Hrs	80 cd/m <sup>2</sup> , 50% checkerboard	Note (3)

Note:

(A) Under V<sub>cc</sub> = 15V, T<sub>a</sub> = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m<sup>2</sup> :

- Contrast setting : 0x9b
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 90 cd/m<sup>2</sup> :

- Contrast setting : 0x77
- Frame rate : 105Hz
- Duty setting : 1/128

(3) Setting of 80 cd/m<sup>2</sup> :

- Contrast setting : 0x60
- Frame rate : 105Hz
- Duty setting : 1/128

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CC}$	Driver power supply (for OLED panel)	-	14.5	15	15.5	V
$V_{CI}$	Low voltage power supply	-	2.6	-	3.5	V
$V_{OH}$	High logic output level	$I_{out}=100\ \mu A$ ,	$0.9 \cdot V_{CI}$	-	$V_{CI}$	V
$V_{OL}$	Low logic output level	$I_{out}=100\ \mu A$ ,	0	-	$0.1 \cdot V_{CI}$	V
$V_{IH}$	High logic input level	$I_{out}=100\ \mu A$ ,	$0.8 \cdot V_{CI}$	-	$V_{CI}$	V
$V_{IL}$	Low logic input level	$I_{out}=100\ \mu A$ ,	0	-	$0.2 \cdot V_{CI}$	V
$I_{CC}$	$V_{CC}$ Supply Current	$V_{CI} = 3.5V$ , $V_{CC} = 18V$ , Display ON, No panel attached, contrast = FF	External $V_{DD} = 2.5V$	600	750	uA
			Internal $V_{DD} = 2.5V$	600	750	
$I_{CI}$	$V_{CI}$ Supply Current	$V_{CI} = 3.5V$ , $V_{CC} = 18V$ , Display ON, No panel attached, contrast = FF	External $V_{DD} = 2.5V$	35	50	uA
			Internal $V_{DD} = 2.5V$	95	120	
$I_{SEG}$	Segment output current Setting $V_{CC}=18V$ , $I_{REF}=10\ \mu A$	Contrast=FF	-	300	370	uA
		Contrast=AF	-	206	-	uA
		Contrast=7F	-	150	-	uA
		Contrast=3F	-	75	-	uA
		Contrast=1F	-	37.5	-	uA

## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	32	34	mA	All pixels on
Standby mode current consumption	-	3	4	mA	Standby mode 10% pixels on
Normal mode power consumption	-	480	510	mW	All pixels on
Standby mode power consumption	-	45	60	mW	Standby mode 10% pixels on
Pixel Luminance	70	90		cd/m <sup>2</sup>	Display Average
Standby Luminance		20		cd/m <sup>2</sup>	
CIE <sub>x</sub> (White)	0.24	0.28	0.32		CIE1931
CIE <sub>y</sub> (White)	0.28	0.32	0.36		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x77
- Frame rate : 105Hz
- Duty setting : 1/128

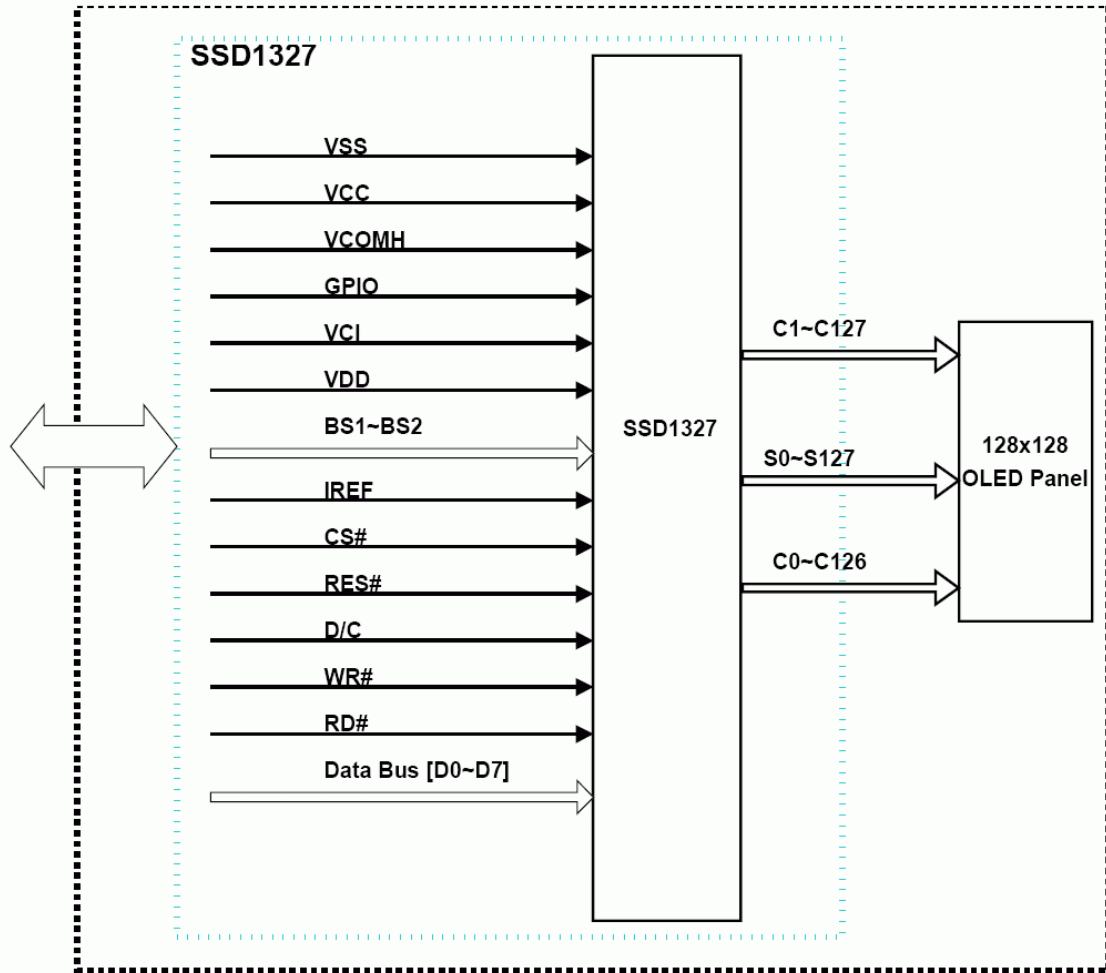
Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x14
- Frame rate : 105Hz
- Duty setting : 1/128



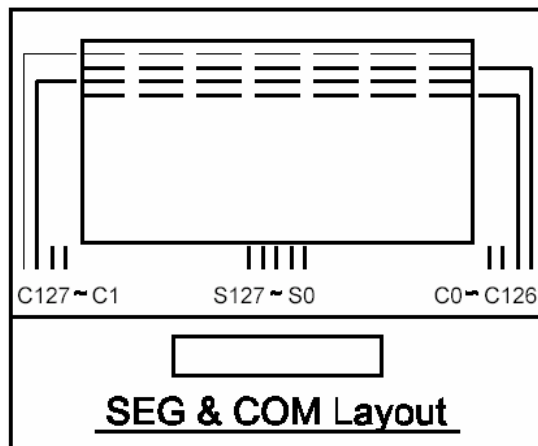
## 7. INTERFACE

### 7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128X128 OLED Module

### 7.2 PANEL LAYOUT DIAGRAM



### 7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground.
VCC	2	Power supply for analog circuit.
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and $V_{SS}$ .
GPIO	4	General I/O port.
VCI	5	Power supply for logic circuit.
VDD	6	A capacitor should be connected between this pin and $V_{SS}$ .
BS1	7	MCU bus interface selection pins.
BS2	8	MCU bus interface selection pins.
VSS	9	Ground.
IREF	10	Reference current input pin. A resistor should be connected between this pin and $V_{SS}$ .
CS#	11	Chip select input.
RES#	12	Reset signal input. When it's low, initialization of SSD1327 is executed.
D/C	13	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
WR#	14	MCU interface input. Data write operation is initiated when it's pull low.
RD#	15	MCU interface input. Data read operation is initiated when it's pull low.
D0	16	Data bus(for parallel interface)
D1	17	
D2	18	
D3	19	
D4	20	
D5	21	
D6	22	
D7	23	
VCC	24	Power supply for analog circuit.
VSS	25	Ground.

### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 ... D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

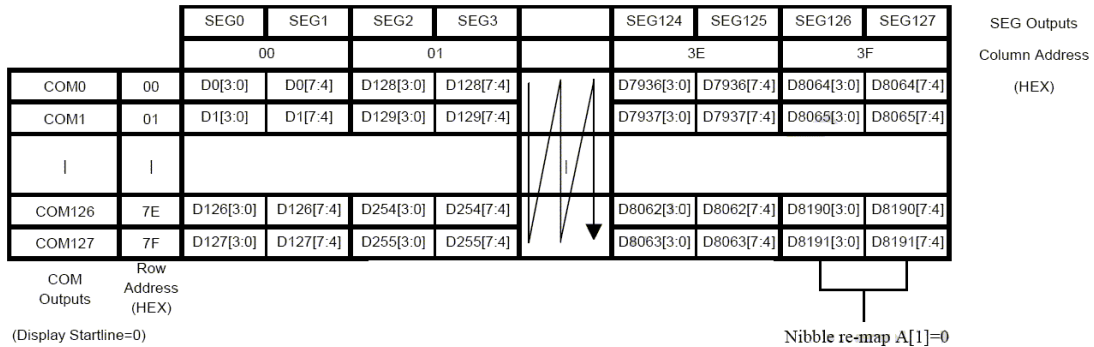
SEG Outputs  
Column Address  
(HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:  
 Disable Column Address Re-map (A[0]=0)  
 Disable Nibble Re-map (A[1]=0)  
 Enable Vertical Address Increment (A[2]=1)  
 Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

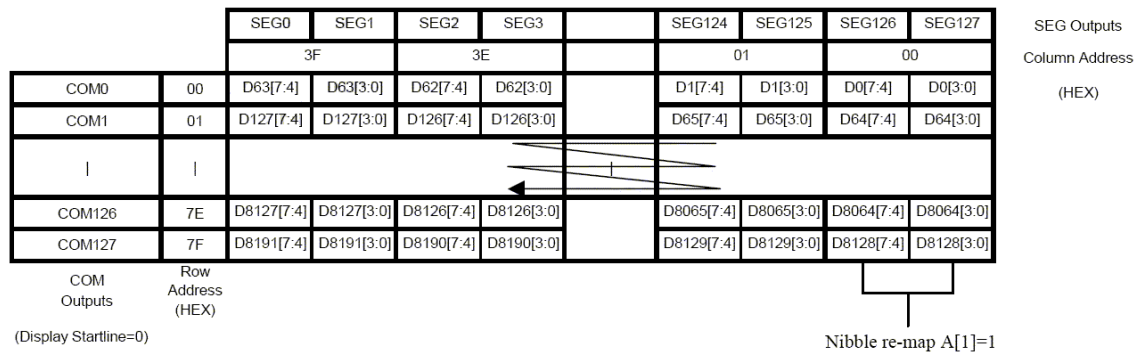
**GDDRAM address map 2**



The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:  
 Enable Column Address Re-map (A[0]=1)  
 Enable Nibble Re-map (A[1]=1)  
 Enable Horizontal Address Increment (A[2]=0)  
 Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

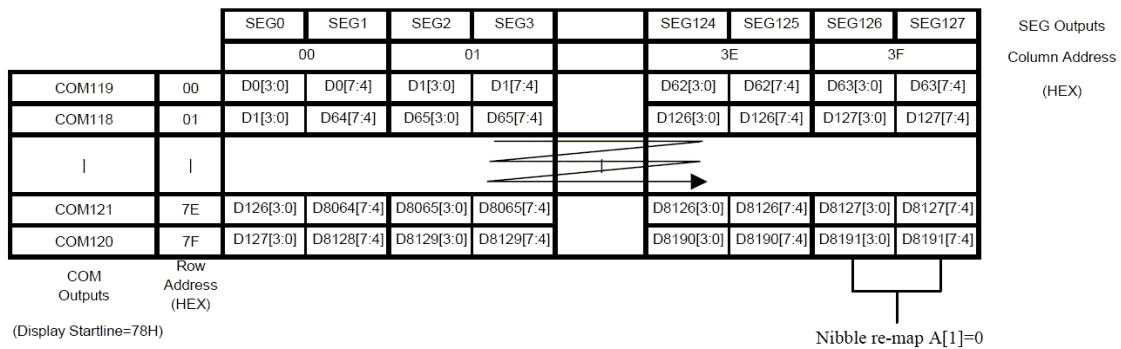
**GDDRAM address map 3**



The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:  
 Disable Column Address Re-map (A[0]=0)  
 Disable Nibble Re-map (A[1]=0)  
 Enable Horizontal Address Increment (A[2]=0)  
 Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 ... D8191

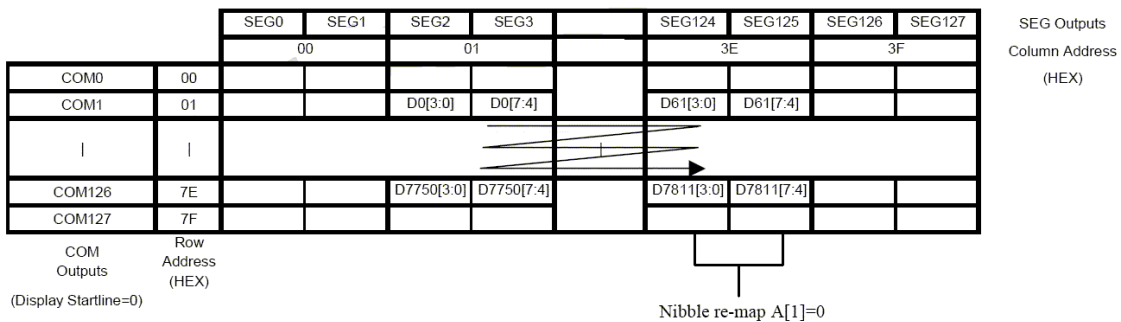
GDDRAM address map 4



The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:  
 Disable Column Address Re-map (A[0]=0)  
 Disable Nibble Re-map (A[1]=0)  
 Enable Horizontal Address Increment (A[2]=0)  
 Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 ... D7811

GDDRAM address map 5



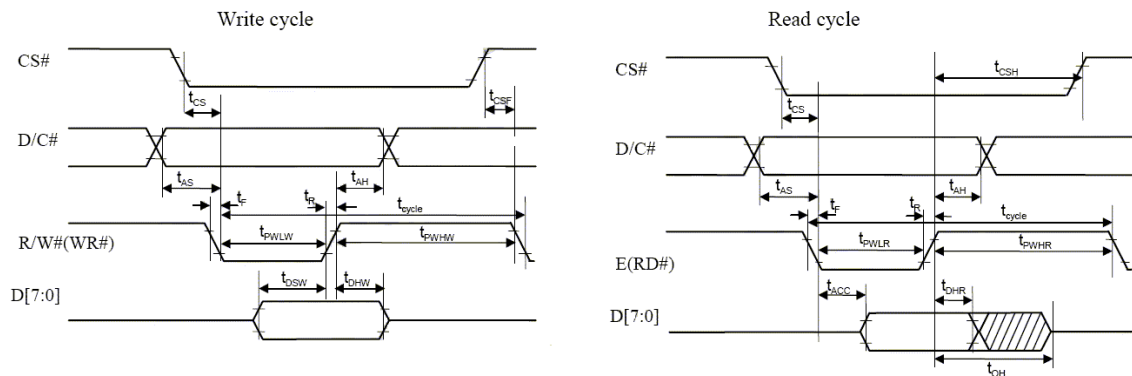
## 7.5 INTERFACE TIMING CHART

### 8080-Series MCU Parallel Interface Timing Characteristics

( $V_{DD} - V_{SS} = 2.4$  to  $2.6V$ ,  $V_{CI} = 3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLR}$	Read Low Time	150	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHR}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

### 8080-series MCU parallel interface characteristics



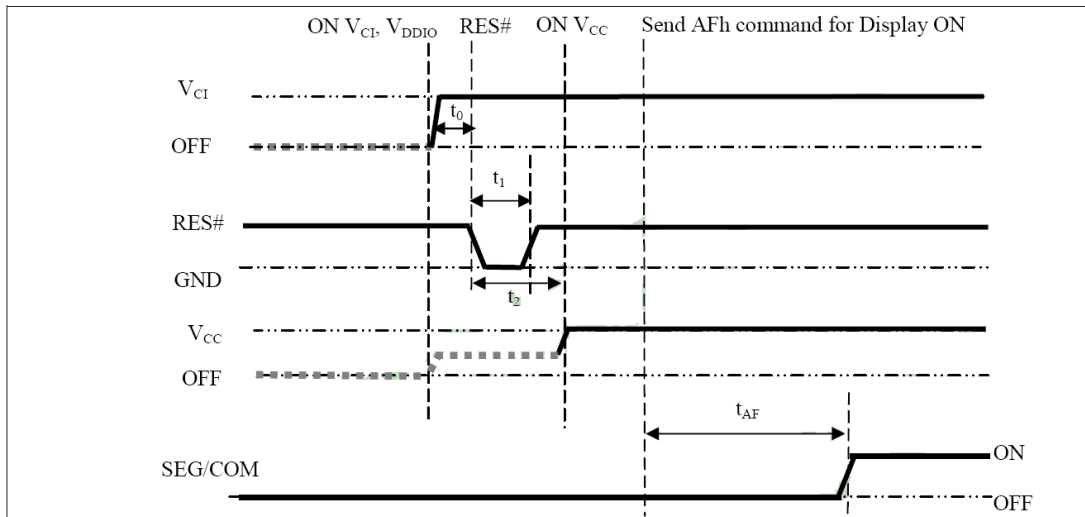
## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

### 8.1 POWER ON / OFF SEQUENCE

#### Power ON sequence:

1. Power ON  $V_{CI}$ .
2. After  $V_{CI}$  becomes stable, set wait time at least 1ms ( $t_0$ ) for internal  $V_{DD}$  become stable. Then set RES# pin LOW (logic low) for at least 100us ( $t_1$ )<sup>(4)</sup> and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us ( $t_2$ ). Then Power ON  $V_{CC}$ .<sup>(1)</sup>
4. After  $V_{CC}$  become stable, send command AFh for display ON. SEG/COM will be ON after 200ms( $t_{AF}$ ).

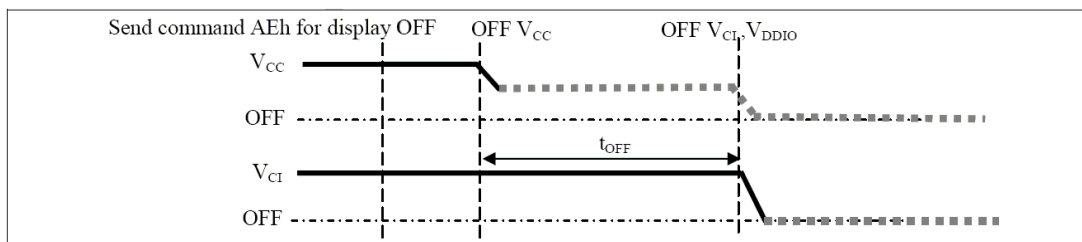
The Power ON sequence.



#### Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF  $V_{CC}$ .<sup>(1), (2), (3)</sup>
3. Wait for  $t_{OFF}$ . Power OFF  $V_{CI}$ . (where Minimum  $t_{OFF}=80ms$ <sup>(5)</sup>, Typical  $t_{OFF}=100ms$ )

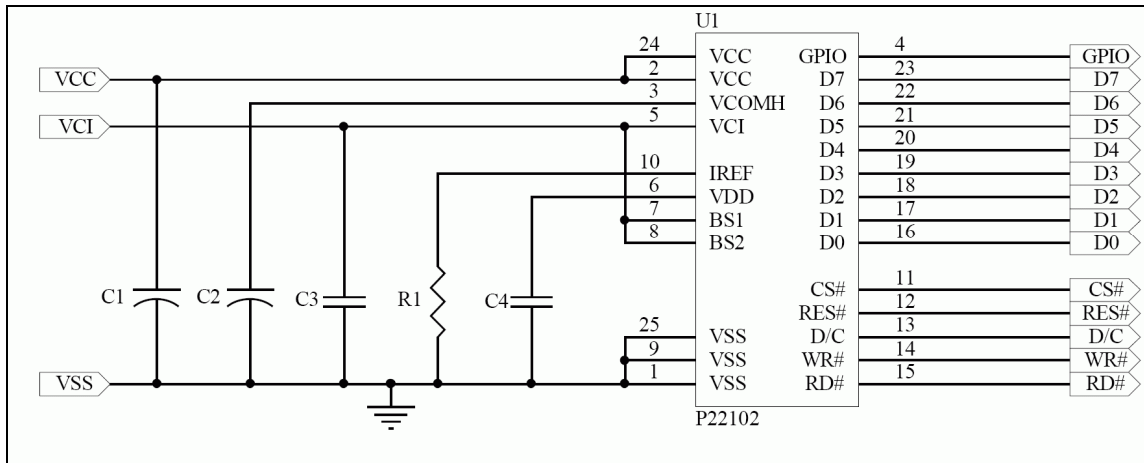
The Power OFF sequence



#### Note:

- (1) Since an ESD protection circuit is connected between  $V_{CI}$  and  $V_{CC}$ ,  $V_{CC}$  becomes lower than  $V_{CI}$  whenever  $V_{CI}$  is ON and  $V_{CC}$  is OFF as shown in the dotted line of  $V_{CC}$  in above figures.
- (2)  $V_{CC}$  should be kept disable when it is OFF.
- (3) Power pins ( $V_{CI}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- (4) The register values are reset after  $t_1$ .
- (5)  $V_{CI}$  should not be Power OFF before  $V_{CC}$  Power OFF

## 8.2 APPLICATION CIRCUIT



### Component:

C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C3, C4: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

**This circuit is for 8080 8bits interface.**

## 8.3 COMMAND TABLE

Refer to IC Spec.: SSD1327



## **9. RELIABILITY TEST CONDITIONS**

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces  Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

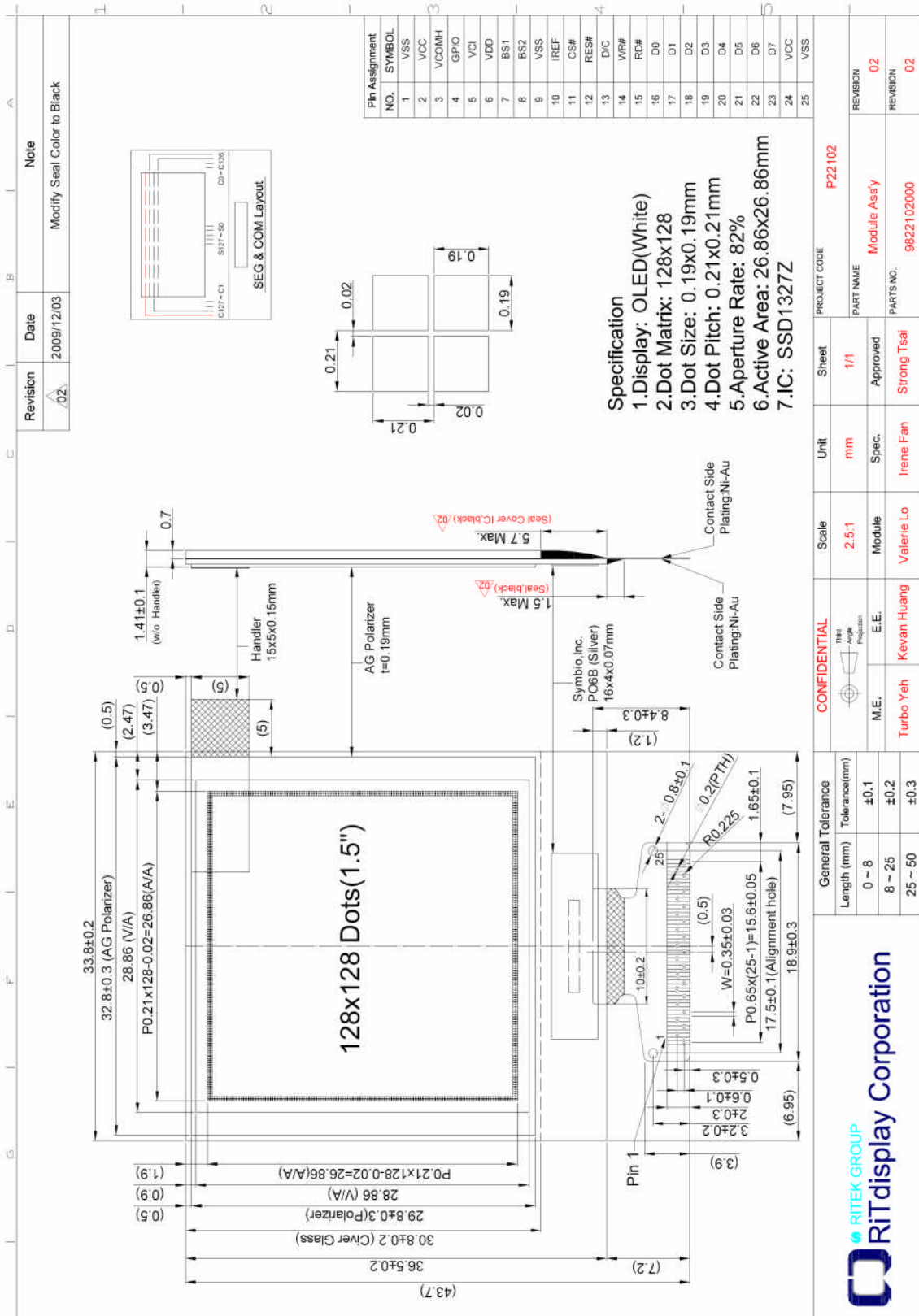
### **Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

### **Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within  $\pm$  50% of initial value.

### 10. EXTERNAL DIMENSION



**11. PACKING SPECIFICATION**

Revision	Date	Note
01	2009/12/07	Packing Tray Instruction

**1** 9822102000 Module Ass'y For P22102 x30 pcs  
**2** Face up ,Rotate packing  
 面朝上,旋轉放置  
**3** 3008000362 Tray 330x270x8.7mm T=0.7mm, PS,P22102  
**4** 3003000012 Vacuum Bag ONY/LDPE 真空包裝袋 ONY/LDPE 480X285x90  
**5** 3003000016 Antistatic Bubble bag 440x(350+450)mm 抗靜電氣泡袋  
**6** 3001000005 Pizza Box 345x285x88,B corrugated B 浪  
**7** 3000000009 Carton 385x305x203mm  
**8** 3006000000 Label 標籤  
**9** 3208000125 Tape 膠帶

**3010000002** 3010000002 5G 矽膠劑 5G 矽膠劑  
**3008000362** Tray =21 pcs 膠帶 3208000125  
 Vacuum packing : 4 sec 抽真空:4秒  
 Rotate stack 旋轉堆疊

ITEM	PART No.	DESC	QTY
1	9822102000	Module Ass'y For P22102	1
2	3008000362	Tray 330x270x8.7 T:0.7mm PS P22102	1200
3	3010000002	5G Silica Gel Desiccants	42
4	3003000012	Vacuum Bag ONY/LDPE 480X285x90	8
5	3003000016	Antistatic Bubble bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88,B corrugated	2
7	3000000009	Carton 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	Tape, W=48mm, L=910cm	3

General Tolerance		Scale		Unit		Sheet	
Length (mm)	0 ~ 8	1:15	Module	mm	Spec.	1/1	Approved
	8 ~ 25		E.E.				Strong Tsal
	25 ~ 50		M.E.				Irene Fan
			T.M.E.				Kelly Hsu
							Allan Yang
							Turbo Yeh
							CONFIDENTIAL
							PROJECT CODE
							P22102
							PART NAME
							Packing Tray Instruction
							VERSION
							01
							PARTS NO.
							9922102000
							VERSION
							01

**RITEK GROUP**  
**RiTdisplay Corporation**

## **12. APPENDIXES**

### **APPENDIX 1: DEFINITIONS**

#### **A. DEFINITION OF CHROMATICITY COORDINATE**

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

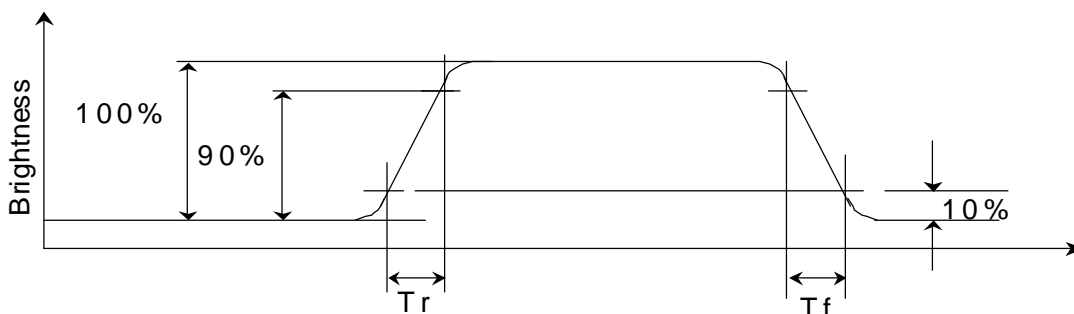
#### **B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

#### **C. DEFINITION OF RESPONSE TIME**

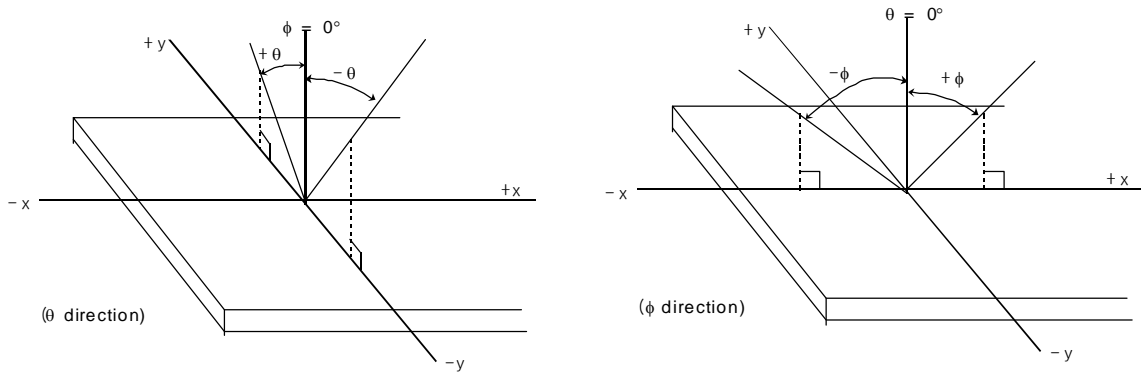
The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.



**Figure 2 Response time**

#### D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

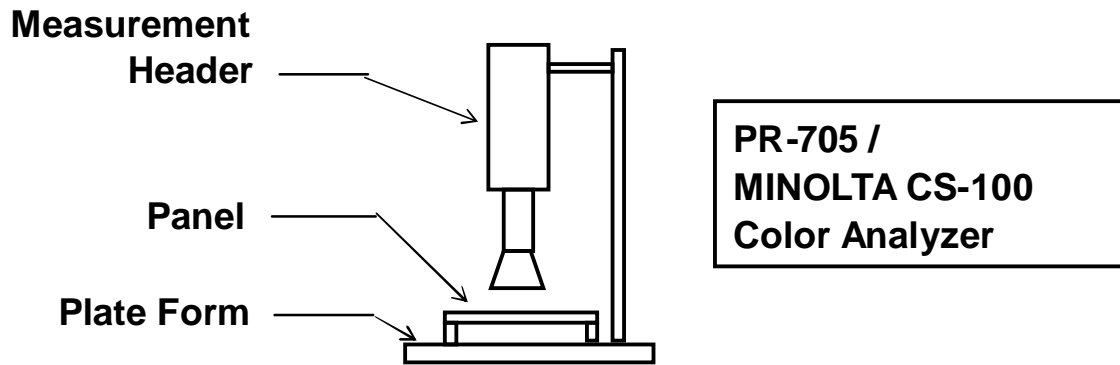


**Figure 3 Viewing angle**

## APPENDIX 2: MEASUREMENT APPARATUS

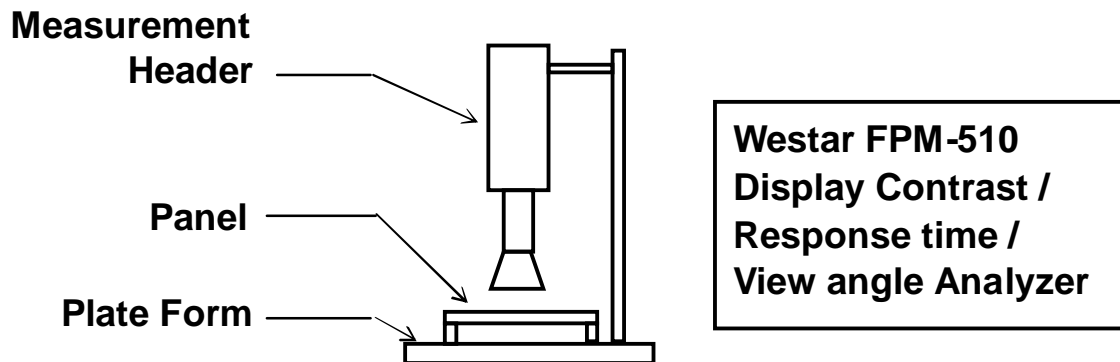
### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

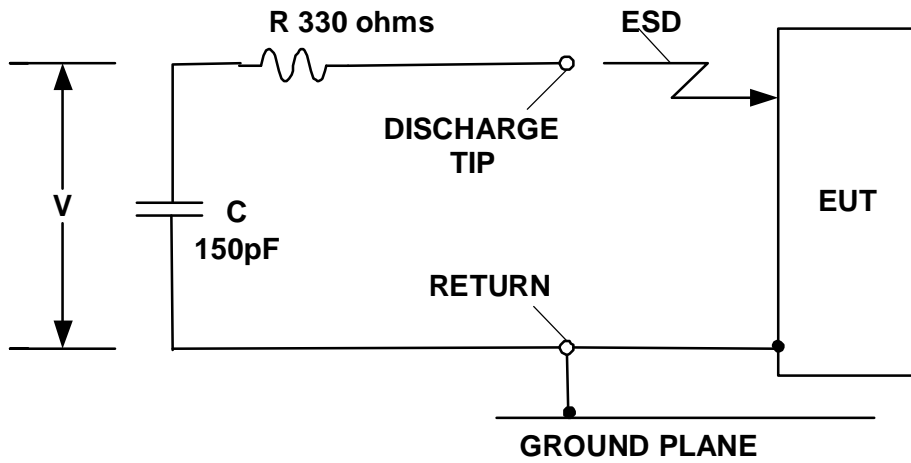


### B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



### C. ESD ON AIR DISCHARGE MODE



## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.