



中显液晶  
技术资料



# 中显RA8820A控制器使用说明书

## ZX240128R

2009年3月15日

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## **1. Module Classification Information**

Z X 2 4 0 1 2 8 R - T M I - V

① ② ③ ④ ⑤ ⑥ ⑦ ⑧

- ① Brand : ZX DISPLAY CORPORATION
- ② Display Type : H→Character Type, G→Graphic Type
- ③ Display Font : 240 x 128dots
- ④ Model serials no.
- ⑤ Backlight Type :
  - N→Without backlight
  - B→EL, Blue green                      A→LED, Amber
  - D→EL, Green                              R→LED, Red
  - W→EL, White                              O→LED, Orange
  - F→CCFL, White                          G→LED, Green
  - Y→LED, Yellow Green                  T→LED, White
- ⑥ LCD Mode :
  - B→TN Positive, Gray                  T→FSTN Negative
  - N→TN Negative,
  - G→STN Positive, Gray
  - Y→STN Positive, Yellow Green
  - M→STN Negative, Blue
  - F→FSTN Positive
- ⑦ LCD Polarize Type/ Temperature range/ View direction
  - A→Reflective, N.T, 6:00              H→Transflective, W.T,6:00
  - D→Reflective, N.T, 12:00              K→Transflective, W.T,12:00
  - G→Reflective, W. T, 6:00              C→Transmissive, N.T,6:00
  - J→Reflective, W. T, 12:00              F→Transmissive, N.T,12:00
  - B→Transflective, N.T,6:00              I→Transmissive, W. T, 6:00
  - E→Transflective, N.T,12:00              L→Transmissive, W.T,12:00
- ⑧ Special Code                      V : Build in Negative voltage

## 2.Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

### **3.General Specification**

<b>Item</b>	<b>Dimension</b>	<b>Unit</b>
Number of Characters	240 x 128dots	—
Module dimension	140.0 x 82.0 x 14.3(MAX)	mm
View area	114.0 x 64.0	mm
Active area	107.98 x 57.58	mm
Dot size	0.43 x 0.43	mm
Dot pitch	0.45 x 0.45	mm
LCD type	STN Negative, Transmissive, Blue	
Duty	1/128	
View direction	6 o'clock	
Backlight Type	LED, White	

### **4.Absolute Maximum Ratings**

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	$T_{OP}$	-20	—	+70	°C
Storage Temperature	$T_{ST}$	-30	—	+80	°C
Input Voltage	$V_I$	$V_{SS}$	—	$V_{DD}$	V
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-0.3	—	+4.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	0	—	30	V
Negative Voltage Output	$V_{EE}$	—	23	—	V
LED Forward Current	$I_F$	—	900	—	mA

\*1 : Operaring on Humidity 90%,the LCM can stand 96 hours no damage.

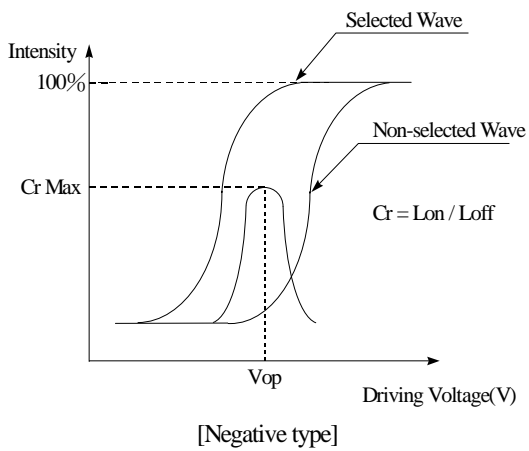
## 5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.5	5.0	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=-20^{\circ}\text{C}$	—	—	21.5	V
		$T_a=25^{\circ}\text{C}$	—	19.3	—	V
		$T_a=+70^{\circ}\text{C}$	17.8	—	—	V
Input High Volt.	$V_{IH}$	—	$0.7 V_{DD}$	—	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	—	0	—	$0.2 V_{DD}$	V
Output High Volt.	$V_{OH}$	—	$0.7 V_{DD}$	—	$V_{DD}$	V
Output Low Volt.	$V_{OL}$	—	0	—	$0.2 V_{DD}$	V
Supply Current	$I_{DD}$	$V_{DD}=5\text{V}$	35.0	45.0	55.0	mA

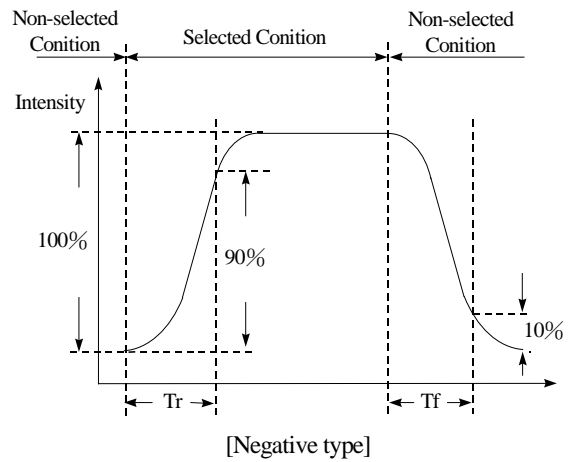
## 6.Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) $\theta$	$CR \geq 2$	20	—	40	deg
	(H) $\varphi$	$CR \geq 2$	-30	—	30	deg
Contrast Ratio	CR	—	—	5	—	—
Response Time	T rise	—	—	150	200	ms
	T fall	—	—	150	200	ms

**Definition of Operation Voltage (Vop)**



**Definition of Response Time (Tr, Tf)**



**Conditions :**

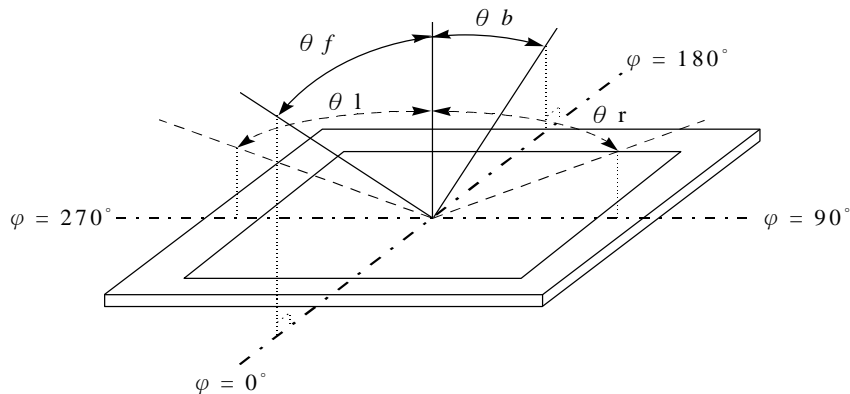
Operating Voltage :  $V_{op}$

Viewing Angle( $\theta$  ,  $\varphi$ ) :  $0^\circ$  ,  $0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty , 1/a bias

**Definition of viewing angle( $CR \geq 2$ )**

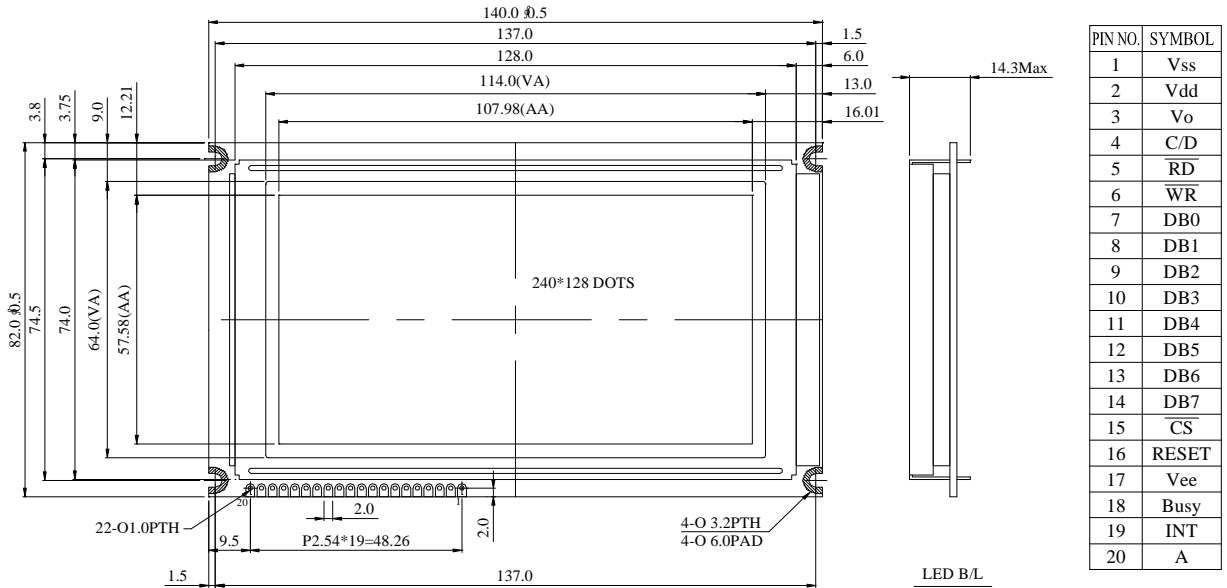


**7.Interface Description**

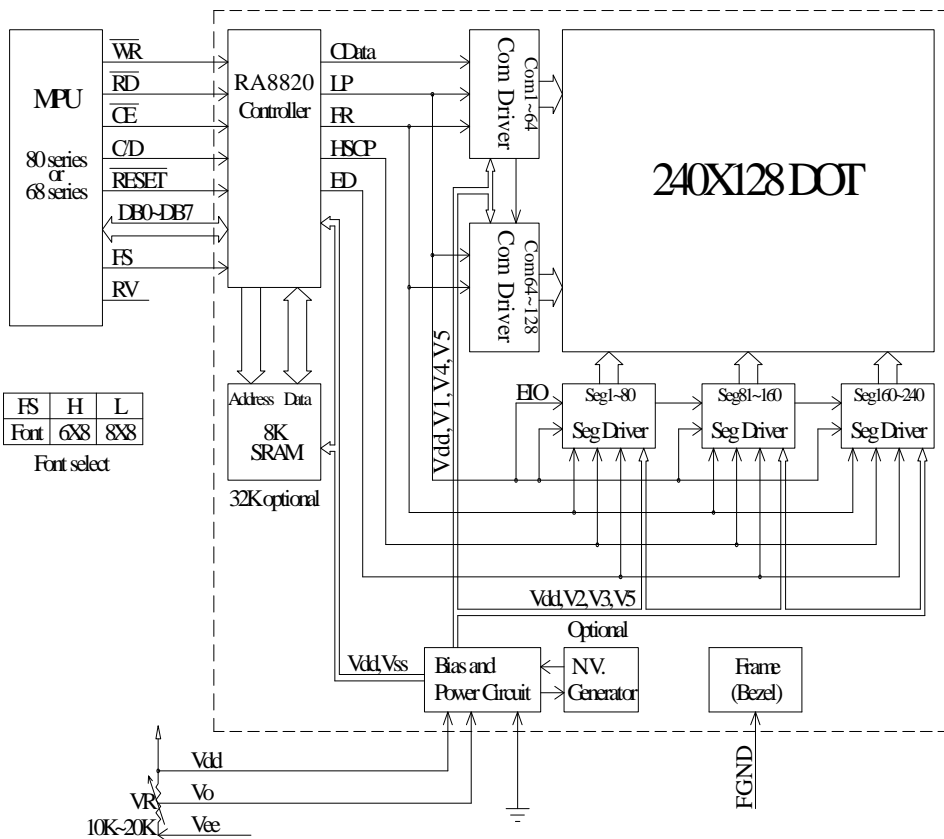
Pin No.	Symbol	Level	Description
1	V <sub>ss</sub>	—	GND
2	V <sub>dd</sub>	—	Power supply ( +5.0 V )
3	V <sub>o</sub>	—	Power supply for LCD driver
4	C/D	H / L	WR=L, C/D=H : Command Write C/D=L: Data write RD=L, C/D=H : Status Read C/D=L: Data read
5	/RD	L	Data read. Read data from RA8820 when RD = L
6	/WR	L	Data write. Write data into RA8820 when WR = L
7	DB0	H / L	Data bus line
8	DB1	H / L	Data bus line
9	DB2	H / L	Data bus line
10	DB3	H / L	Data bus line
11	DB4	H / L	Data bus line
12	DB5	H / L	Data bus line
13	DB6	H / L	Data bus line
14	DB7	H / L	Data bus line
15	/CS	L	L : Chip enable
16	/RESET	H / L	H : Normal ; L : Initialize RA8820
17	V <sub>ee</sub>	—	Negative voltage output
18	BUSY	H / L	Active high or low busy signal. The RA8820 can't be access when BUSY pin is high. It's should be connected to MPU I/O input. The MPU have to poll this pin before accessing RA8820.
19	INT	—	Active high or low Interrupt signal
20	A	—	Power Supply For LED +



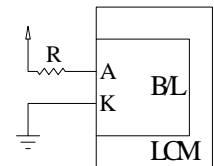
# 8. Contour Drawing & Block Diagram



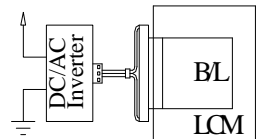
The non-specified tolerance of dimension is ±0.3 mm .



LEDB/L drive directly from A,K.



CCFL B/L drive directly from connector.



External contrast adjustment.

## 9. Register Description

### 9.1 Register List Table

Reg. No	Reg. Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	LCR	R/W	PW1	PW2	SR	RTM	CG	DP	DK	DV
08h	MIR	R/W	ABP	CKN	DISP	PLR	--	--	CKB1	CKB0
10h	CCR	R/W	ARI	ALG	WDI	WBC	AIX	CP	CK	CSD
18h	CSCR	R/W	CR3	CR2	CR1	CR0	DY3	DY2	DY1	DY0
20h	AWRR	R/W	--	--	X5	X4	X3	X2	X1	X0
28h	DWRR	R/W	--	--	A5	A4	A3	A2	A1	A0
30h	AWBR	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
38h	DWBR	R/W	B7	B6--	B5	B4	B3	B2	B1	B0
40h	AWLR	R/W	--	--	SS5	SS4	SS3	SS2	SS1	SS0
48h	DWLR	R/W	--	--	C5	C4	C3	C2	C1	C0
50h	AWTR	R/W	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
58h	DWTR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
60h	CPXR	R/W	--	--	RS5	RS4	RS3	RS2	RS1	RS0
70h	CPYR	R/W	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
80h	BTR	R/W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0
90h	SCCR	R/W	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0
A0h	INTR	R/W	BSY	INA	INX	INY	MSZ	MSA	MSX	MSY
B0h	INTX	R/W	--	--	IX5	IX4	IX3	IX2	IX1	IX0
B8h	INTY	R/W	IY7	IY6	IY5	IY4	IY3	IY2	IY1	IY0
C0h	TPCR	R/W	AZEN	AZOE	--	ADET	AS3	AS2	AS1	AS0
C8h	TPDR	R	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
D0h	LCCR	R/W	DZEN	DZWE	DRST	DAC4	DAC3	DAC2	DAC1	DAC0
E0h	PDR	R/W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F0h	FCR	R/W	TNS	BNK	RM1	RM0	FDA	ASC	ABS1	ABS0

## 9.2 Register Description

### REG [00h] LCD Controller Register (LCR)

Bit	Description	Text/Graph	Default	Access
7-6	<p>Power Mode            11: Normal Mode            10: Standby Mode            01: Sleep Mode            00: Off Mode</p> <p><b>Normal mode:</b> When RA8820 is in normal mode it can execute full functions include RAM read/write, register read/write, LCD display valid signal.</p> <p><b>Standby mode:</b> When RA8820 is in standby mode, except DDRAM/ROM access function is prohibited, others are working and so does LCD display function.</p> <p><b>Sleeping mode:</b> When RA8820 is in sleeping mode, the DDRAM/ROM access and LCD display are prohibited, but register access is permitted.</p> <p><b>Off mode:</b> When RA8820 is in off mode, all above functions enter poweroff mode, except the wake-up trigger block. If wake-up event occurred, HT8820 would wake-up and return to Normal mode.</p>	--	11h	R/W
5	<p>Software Reset:            1: Reset all registers except flushing RAM            0: Normal operation</p>		0h	R/W
4	<p>Set Auto_reset function            When the bit is Enable, if RA8820 doesn't get a full command or data within 2msec, then HT8820 will ignore it.            1: Enable Auto_reset function            0: Disable Auto_reset function</p>		0h	R/W
3	<p>Display mode selection            1: Character mode            The written data will be treated as a GB/BIG/ASCII code.            0: Graphical mode            The written data will be treated as a bit-map pattern.</p>		1h	R/W
2	<p>Set Display on or off. The bit can control LCD Driver Interface signals            DISP_OFF signal control            1: DISP_OFF pin output high            0: DISP_OFF pin output low.</p>	Text/Graph	1h	R/W
1	<p>Blink mode selection            0: Normal display            1: Blink full screen. The blink time is set by CBTR.</p>	Text/Graph	0h	R/W
0	<p>Inverse mode selection            1: Normal display            0: Inverse full screen. It will cause all data stored in DDRAM inversed.</p>	Text/Graph	1h	R/W

**REG [10h] Cursor Control Register (CCR)**

Bit	Description	Text/Graph	Default	Access
7	Auto Increase Cursor Position in reading DDRAM operation. 1: Enable 0: Disable	Text/Graph	1H	R
6	Chinese/English character alignment 1: Enable 0: Disable The bit only valid in character mode, that can align full-size and half-size mixed font	Text	1H	R/W
5	Store Current Data to DDRAM 1: Store Current Data to DDRAM directly 0: Store Current Data to DDRAM Inversely	Text	1H	R/W
4	Set Bold font (character mode only) 1: Store Data shift 1 + origin data (Black Font) 0: Store Data Normality (origin Font)	Text/Graph	1H	R/W
3	Auto Increase Cursor Position in writing DDRAM operation. 1: Enable 0: Disable	Text/Graph	0H	R/W
2	Cursor display control 1: Set cursor on 0: Set cursor off	Text/Graph	0H	R/W
1	Cursor blink control 1: blink Cursor. The blink time is determined by register[80h] BTR 0: Normal	Text/Graph	0H	R/W
0	Set Cursor width 1: Cursor width is auto adjust by input data 0: Cursor is fixed at one byte width	Text	0H	R/W

**REG [20h] Active Window Right Register (AWRR)**

Bit	Description	Default	Access
7-6	Reserved	0H	R
5-0	Active window right position → Segment-Right	Table 10-2	R/W

**Note:** REG [20h, 30h, 40h, 50h] are used for the function of change line and page. Users can use these four Registers to set a block as an active window. When data goes beyond the right boundary of active window (The value is set by REG [20h, 30h, 40h, 50h]), then the cursor will automatically change the line and write in data continuously. It means the cursor will move to the left boundary of active window, which is set by REG [40h]. When the data comes to the bottom line of the right side (set by REG [20h and 30h]), then the cursor will be moved to the first line of the left side automatically and continue to put in data. (set by REG [40h, 50h]).

**REG [30h] Active Window Left Register (AWBR)**

Bit	Description	Default	Access
7-0	Active window bottom position Common-Bottom	Table 10-1	R/W

**REG [40h] Active Window Bottom Register (AWLR)**

Bit	Description	Default	Access
7-6	Reserved	0H	R

5-0	Active window left position Segment-Left	0H	R/W
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**REG [50h] Active Window Top Register (AWTR)**

Bit	Description	Default	Access
7-0	window top position → Common-Top	0H	R/W

**REG [60h] Cursor Position X Register (CPXR)**

Bit	Description	Default	Access
7-6	Reserved	0H	R
5-0	Set the cursor Segment address	0H	R/W

**REG [70h] Cursor Position Y Register (CPYR)**

Bit	Description	Default	Access
7-0	the cursor Common address	0H	R/W

**REG [80h] Cursor Blink Time Register (BTR)**

Bit	Description	Text/Graph	Default	Access
7-0	The Blink one unit time scale is the frame rate scale Blinking time = Bit [7..0] x (1/Frame_Rate) Frame Rate setup depends on the LCD panel.	Text/Graph	23H	R/W

**REG [90h] Shift Clock Control Register (SCCR)**

Bit	Description	Default	Access
7-0	Setup the XCK signal cycle <b>OCKR = (SCLK*4)/(Column*Row*FRS)</b> SCLK: System Clock (Hz) DBW: 4(Bit) Column: Column of Display Screen (Pixel) Row: Row of Display Screen (Pixel) FRS: Frame Rate/Sec <b>Note: OCKR initial setup</b> <b>OCKR=MA[7..0] during reset period.</b>	Table10-2	R/W

**REG [A0h] Interrupt Setup & Status Register (INTR)**

Bit	Description	Default	Access
7	Busy Status 1: HT8820 is busy. The MPU have to wait until Busy Status is released 0: HT8820 is idle ready for MPU access.	Table10-2	R/W
6	Touch Panel detect 1: Touch Panel touched 0: Touch Panel untouched	0H	R
5	Cursor Column status 1: The Cursor Column is equal to INTX 0: The Cursor Column is not equal to INTX	0H	R
4	Cursor Row status 1: The Cursor Row is equal to INTY 0: The Cursor Row is not equal to INTY	0H	R
3	Busy interrupt mask 1: Enable Busy to generate Interrupt output 0: Disable Busy to generate Interrupt output	0H	R
2	Touch Panel interrupt mask 1: Generate interrupt output if touch panel was detected. 0: Don't generate interrupt output if touch panel was detected.	0H	R/W
1	INTX event occur INT or not 1: Enable INTX Interrupt 0: Disable INTX Interrupt	0H	R/W
0	Set INTY occur INT or not 1: Enable INTY Interrupt 0: Disable INTY Interrupt	0H	R/W

**REG [B0h] Interrupt Column Setup Register (INTX)**

Bit	Description	Default	Access
7-6	Reserved	0H	R
5-0	Setup interrupt column address If Cursor Position X Register (CPXR)=INTX, a interrupt has occurred	27H	R/W

**REG [B8h] Interrupt Row Setup Register (INTY)**

Bit	Description	Default	Access
7-0	Setup interrupt Row address If Cursor Position Y Register (CPYR)=INTY, a interrupt has occurred	EFh	R/W

**REG [C8h] Touch Panel Data Register (TPDR)**

Bit	Description	Default	Access
7-0	This register keeps the touch panel active position (Column, Row)	0H	R

**REG [D0] LCD Contrast Control Register (LCCR)**

Bit	Description	Default	Access
7	LCD contrast control 1: Disable 0: Enable	1H	R/W
6	LCD contrast control DAC write enable 1: Don't allow MPU to write data to DAC Bit [4~0] 0: Allow MPU to write data to DAC Bit [4~0]	1H	R/W
5	Reset LCD contrast control function 1: Normal operation 0: DAC is reset. Set the Iout to 0 uA	1H	R/W
4-0	Set the LCD Brightness Control Iout Value (DAC Bit [4~0]) 00000b 0uA (Min. Current) : : 11111b 1mA (Max. Current)	0H	R/W

**REG [E0h] Pattern Data Register (PDR)**

Bit	Description	Text/Graph	Default	Access
7-0	Setup the Pattern Data When REG[F0h] bit3 is '1', it will read the data from Register [E0h] and fill the whole DDRAM. After the movement of filling the Active window, REG[F0h] bit3 will become "0".	Graph	0H	R/W

**REG [F0h] Font Control Register (FCR)**

Bit	Description	Text/Graph	Default	Access
7	External Character ROM control 1: Enable. 0: Disable.		01H	R/W
6	ROM BANK Selection 1: External Font ROM select 0: Internal Font ROM select		00H	R/W
5-4	Set Font ROM Translate 01: Support BIG5 font ROM 10: Support GB font ROM		00H	R/W
3	Fill Data to DDRAM 1: no action 0: Fill Data to DDRAM Enable	Graph	00H	R/W
2	Font ROM range select 1: Enable 0: Disable When the bit is '1', input data is ASCII code When the bit is '0', the input data <A0h it is as ASCII code		00H	R/W

	code the input data ≡ A0h it is as GB/BIG5 Enable CLK_OUT1: Active_window			
1-0	ASCII Block Select bit 1~0 0 0: Map to ASCII block 0 0 1: Map to ASCII block 1 1 0: Map to ASCII block 2 1 1: Map to ASCII block 3		00H	R/W

**REG [08h] Misc. Register (MIR)**

Bit	Description	Default	Access
7	Reserved	1H	R
6	ENABLE CLK_OUT 1: Enable CLK_OUT 0: Disable CLK_OUT	1H	R/W
5	Window Mode Select 1: Active_window 0: Display_window	0H	R/W
4	Set INT and Busy Polarity 1: Set High_Active mode 0: Set Low_Active mode	0H	R/W
3-2	<b>Reserved</b>	0H	R
1-0	Clock speed selection 0 0 : 1MHz 0 1 : 2MHz 1 0 : 4MHz 1 1 : 8MHz		

**REG [18h] Cursor Size Control Register (CSCR)**

Bit	Description	Text/Graph	Default	Access
7-4	Setup the height of cursor (default value is 2)	TEXT	0010H	R/W
3-0	Setup the distance of row to row	TEXT	0010H	R/W

**REG [28h] Display Window Right Register (DWRR)**

Bit	Description	Default	Access
7-6	Reserved	0H	R/W
5-0	Set Display Window Right position Segment-Right Segment-Right = ( Segment Number / 8 ) - 1 If LCD panel size is 320*240, the value of the register is: ( 320 / 8 ) - 1 = 27h	0H	R/W

Note: REG[28h, 38h, 48h, 58h] is used to set Display Window. Users can set the viewing scope of Display RAM.

Column Address can be set between 0~39, and Row Address can be set between 0~239. Users can set start and end address first, and then by adding shift function to present the effect of rolling.

**REG [38] Display Window Bottom Register (DWBR)**

Bit	Description	Default	Access
7-0	Display Window Bottom position Common-Bottom Common_Bottom = LCD Common Number - 1 If LCD Panel is 320x240, the value of the register is: 240 - 1 = 239 = EFh	Table 10-2	R/W

**REG [48] Display Window Left Register (DWLR)**

Bit	Description	Default	Access
7-0	Display Window Left position → Segment-Left Usually set "00h".	0H	R/W

**REG [58] Display Window Top Register (DWTR)**

Bit	Description	Default	Access
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7-0	Display Window Top position → Common-Top Usually set "00h".	0H	R/W
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## NOTE:

Please look at this example of how to set the default value of the Register.

1.  $AWRR \geq CPXR \geq AWBR$ ,  $AWRR \geq INTX \geq AWBR$
2.  $AWLR \geq CPYR \geq AWTR$ ,  $AWLR \geq INTY \geq AWTR$



## 10. Function Description

### 10.1 MPU Interface

The RA8820 enters 8-bit bus interface mode when the SYS\_DB pin is set high. The RA8820 can interface with the MPU via an I/O port. Instruction is executed when data is written into the register. In this case, only the register can be read (busy check, etc). In this case, check the busy flag when accessing (polling), or appreciate connect Busy pin to MPU Interrupt with the exact polarity it can useful reduce MPU polling effort, or insert an interval considering the execution time and perform the next access when the internal process has completely finished. The instruction execution time depends on the RA8820 operation frequency. When using the internal oscillator circuit of the RA8820, the instruction time will change as the oscillation frequency does.

The RA8820's MPU interface support Intel (8080) or Motorola (6800) 4/8 bits data bus, RA8820 lead the setup data while reset period via LD [7..0].

**Table 10-1 Hardware Pin Setup Description**

Bit	Signal	Description	"1" mean	"0" mean
7	SYS_MI	MPU Type	M6800	I8080
6	SYS_DB	MPU Data Bus	8 bit	4 bit
5	SYS_FQ	Clock Select	PLL_CLK	RC Osc CLK
4	--	--	--	--
3	SYS_LD	LCD Data Bus	8 Bit	4 Bit
2	SYS_PLR	RS Polarity Select	Note1	Note2
1	X1	Operation Mode	Set → "1"	
0	X2			

Note1: '1' indicate DB[7..0] are display data; '0' indicate DB[7..0] are register data

Note2: '1' indicate DB[7..0] are register data; '0' indicate DB[7..0] are display data

### 10.2 Command/Decoder register circuit

This circuit store and implement the command from MPU Interface. The Register [00h, 08h, 10h] treats the whole chip and cursor setup. The Register [20h, 30h, 40h, 50h] can setup the work range maximum and minimum limit. When appreciate setup with Register [10h] bit3, [F0h] bit3 and [60h, 70h] the RA8802 can offer powerful variety meet various application.

The Register [28h, 38h, 48h, 58h] can satisfy various LCD display from (0,0)~(320,240) pixels. Powerful INT via Register [A0h, B0h, B8h] reduce MPU polling cycle to Interrupt interactive utility. Therefore we can use low end CPU to cost down and help the whole system reduce BOM cost.

### 10.3 Busy Flag

The Busy flag is set when the RA8820 is too busy to write RAM data. During operation, RA8820 can accept as normal operation expect write data to display data RAM. RA8820 accepts read status instruction only. The busy flag signal is output at pad DB7 when read status is issued. If the cycle time is correct, the microprocessor need not check the flag before issuing a command. This can greatly improve the microprocessor performance.

## 10.4 INT

When appreciate setup register [A0h, B0h, B8h]. RA8820 can assert INT signal which the cursor go to the interrupt position, it is useful to help system developer to apply two or more RA8820 to driver large panel. example: Panel size is 640×480→Column×Row.

## 10.5 Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores bit mapping pixel data and display attribute codes for displaying data. A fullsize font is displayed using two bytes, and a half-size font is displayed using one byte. DDRAM displays only that data stored within the range corresponding to the DDRAM. Data stored outside the range is ignored. Refer to combined display of full-size and half-size characters for details on character codes stored in DDRAM.

The display data RAM stores pixel data for LCD. It is a 240 column by 320 row addressable array maximum. The time required to transfer data is very short. The microprocessor writes and reads data to/from the RAM through data bus. As the LCD controller operates independently, data can be written into the RAM at the same time as the data is being displayed, without the LCD to flicker. If apply to the character/graphical mix mode. HT8820 can easy store and display the data/picture which user desired.

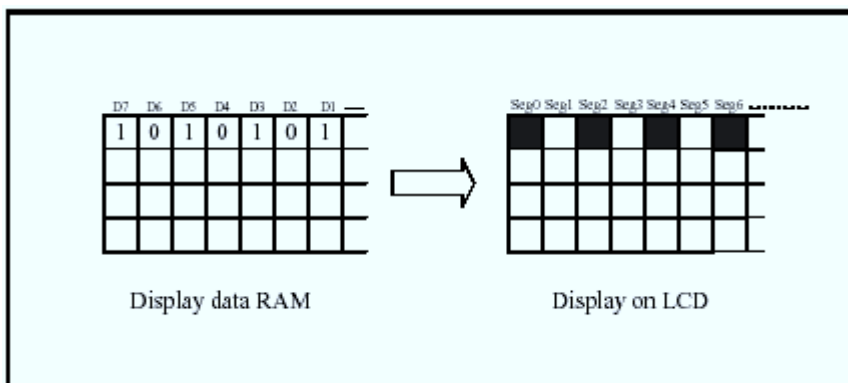


Figure 10-1 Display data to LCD map

## 10.6 Display Timing Generator

This section explains how the display timing generator circuit operates.

### 10.6.1 Signal Generation to Line Counter and Display Data Latch Circuit

The display data clock (XCK) generates a clock to the line counter and a latch signal to the display data latch circuit. The line address of the display RAM is generated in synchronization with the display clock. Display data is latched by the display data latch circuit in synchronization with the display clock and output to the Column LCD drive data bus. The display data is send to the LCD drive circuit completed independent of access to the display data RAM from the microprocessor.

### 10.6.2 LCD AC Signal Generation

The display data clock generates an LCD AC signal (FRM). The FRM causes the LCD drive circuit to generate an AC drive waveform.

### 10.6.3 Row Timing Signal Generation

The display clock generates an internal Row timing signal and a start signal (YD) to the Row driver. A Display clock resulting from frequency division of an oscillation clock is output from the XCK pad.

When an AC signal (FRM) is switched, a high pulse is output as a YD output at the turning edge of the previous display clock.

## 10.7 ROM

HT8820 embedded 512KByte Font ROM also provide external 512KByte Font ROM Interface can use put the standard and special fonts of BIG5, GB, and ASCII code. It can support the display 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display. For example, when CPU sends Big5 code (2 Bytes), RA8802 will read Font code (32 Bytes) from ROM, which is matching with Big5 code, and then deliver them to DDRAM.

Table106-2 Panel Size Initial Setup

MA[11..8]		Seg×Com (Chi-Font)	Seg×Com (Pixel)	REG[20h]	REG[30h]
0	0000	20×15	320×240	27	EF
1	0001	20×10	320×160	27	9F
2	0010	20×8	320×128	27	7F
3	0011	20×4	320×64	27	3F
4	0100	16×8	256×128	1F	7F
5	0101	15×10	240×160	1D	9F
6	0110	15×8	240×128	1D	7F
7	0111	15×4	240×64	1D	3F
8	1000	10×10	160×160	13	9F
9	1001	10×8	160×128	13	7F
A	1010	10×4	160×64	13	3F
B	1011	10×2	160×32	13	1F
C	1100	12×4	192×64	17	3F
D	1101	8×8	128×128	0F	7F
E	1110	8×4	128×64	0F	3F
F	1111	8×2	128×32	0F	1F

Note: When register [20h, 30h] are reset we can utilize Table10-2 to select panel size

### 10.9 DAC

RA8802 includes one 5 bit DAC, providing current to make contrast adjustments. Figure 10-4 is the circuit for voltage adjustment.

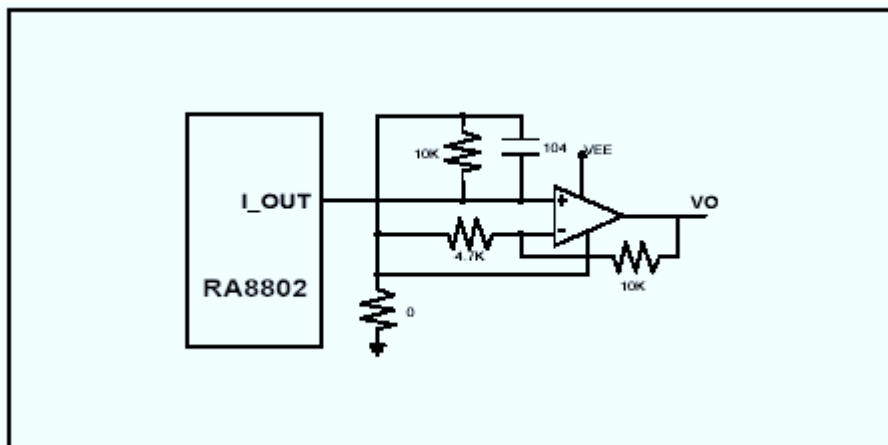


Figure 10-4 DAC Current to Voltage Regulator

# 11. Function Application

## 11.1 Combined Display of Full-Size and Half-Size Characters

The Figure 11-1 shows the ability of RA 8820 to show Full-Size and Half-Size Characters



Figure 11-1 Combined Display of Full-Size and Half-Size Characters

Table 11-1 is the character code of Full-Size and Half-Size showed in Figure 11-1.

Table 11-1 Character Code comparison table (BIG5)

Display Character	Character Code	Display Character	Character Code	Display Character	Character Code
瑞	B7E7	E	45	o	6F
佑	A6F6	C	43	c	63
科	ACEC	H	48	m	6D
技	A7DE	N	4E	t	74
股	AAD1	L	4C	電	20B7
份	A5F7	G	47	話	71B8
有	A6B3	Y	59	8	38
限	ADAD	.	2E	6	36
公	A4BD	網	BAF4	3	33
司	A571	頁	ADB6	5	35
R	52	:	3A	7	37
A	41	w	77	傳	20B6
I	49	r	72	真	C7AF
O	4F	a	61		
T	45	i	69		

## 11.2 Character Bold Display Function

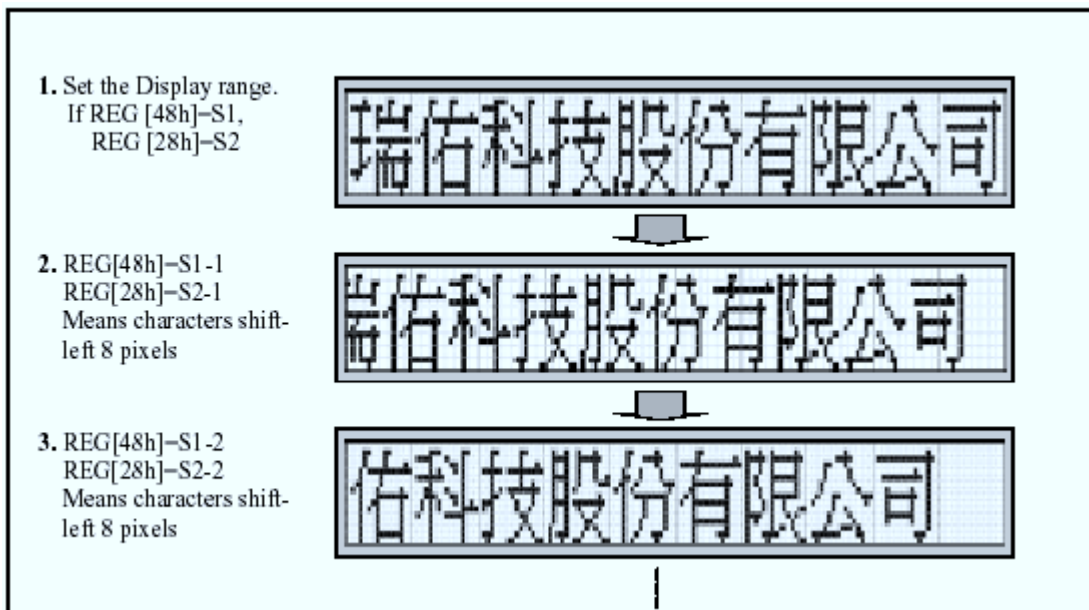
The figure 11-2 is character bold display and Register setup.



Figure 11-2 Character Bold Display

## 11.3 Horizontal Smooth Scroll

Data shown on the display can be scrolled horizontally to the left for a specified number of dots. The number of dots are set in scroll control register [28, 48h].

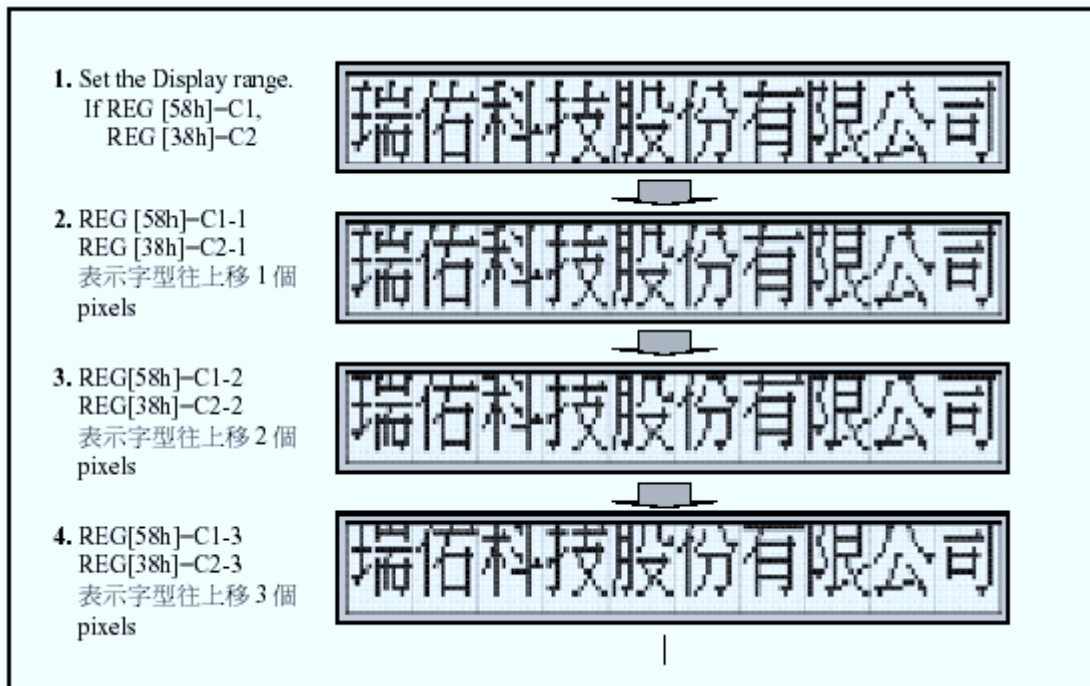


Note: One square means 16\*16 pixels

Figure 11-3 Horizontal Smooth Scroll

### 11.4 Vertical Smooth Scroll

Like Figure 11-4 shows, it can set Active Window. Then setting register to achieve the function of rolling up and down.



**Note:** One square means 16\*16 pixels

Figure 11-4 Vertical Smooth Scroll

### 11.5 Graphics Display Function

Figure 11-5 shows the function and the value that register need be set under graphics display.



Figure 11-5 Graphics Display



## 11.6 Blinking Display

Figure 11-6 shows the function and the value that register need to be set under blinking display.



Figure 11-6 Blinking Display



### 11.7 Black-white Display

Figure11-7shows the function and the value that register need to be set under black-white display.

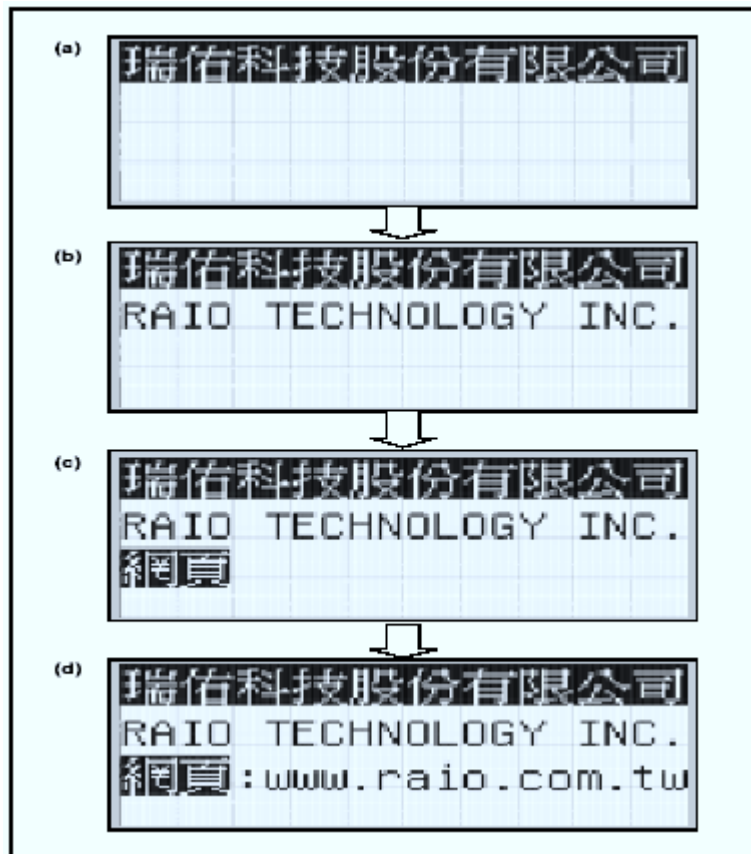


Figure 11-7 Blinking Display

- (a)
1. Set REG [10h] bit5-0
  2. Write in the Big5 code of "瑞佑科技股份有限公司" then it will show up "瑞佑科技股份有限公司"
- (b)
3. Hold on (a)
  4. Set REG [10h] bit5-1
  5. Write in the Big5 code of "RAIO TECHNOLOGY INC." then it will show up " RAIO TECHNOLOGY INC."
- (c)
6. Hold on (a), (b)
  7. Set REG [10h] bit5-0
  8. Write in the Big5 code of "網頁" then it will show up "網頁"
- (d)
9. Hold on (a), (b) and (c)
  10. Set REG [10h] bit5-1
  11. Write in the Big5 code of": www.raio.com.tw" then it will show up ": www.raio.com.tw"

### 11.8 Align the Chinese/English Font

Figure11-8 shows the function and the value that register need to be set under aligning the Chinese/English Font,

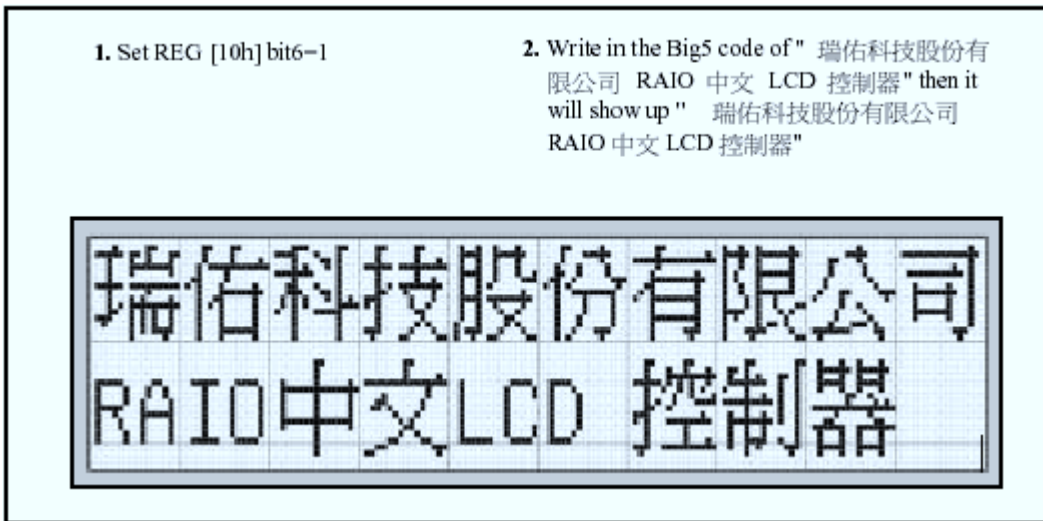


Figure 11-8 Align the Chinese/English Font

### 11.9 Non\_Align the Chinese/English Font

Figure11-9 shows the function and the value that register need to be set under Non\_Align the Chinese/English Font.

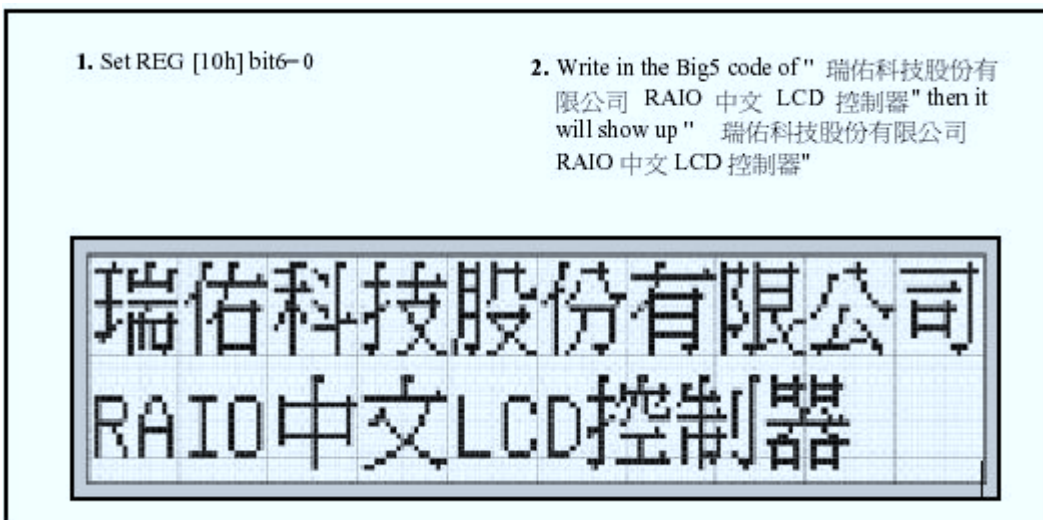


Figure 11-9 Non\_Align the Chinese/English Font

## 12 Timing Characteristics

### 12.1 8080 CPU System Buses

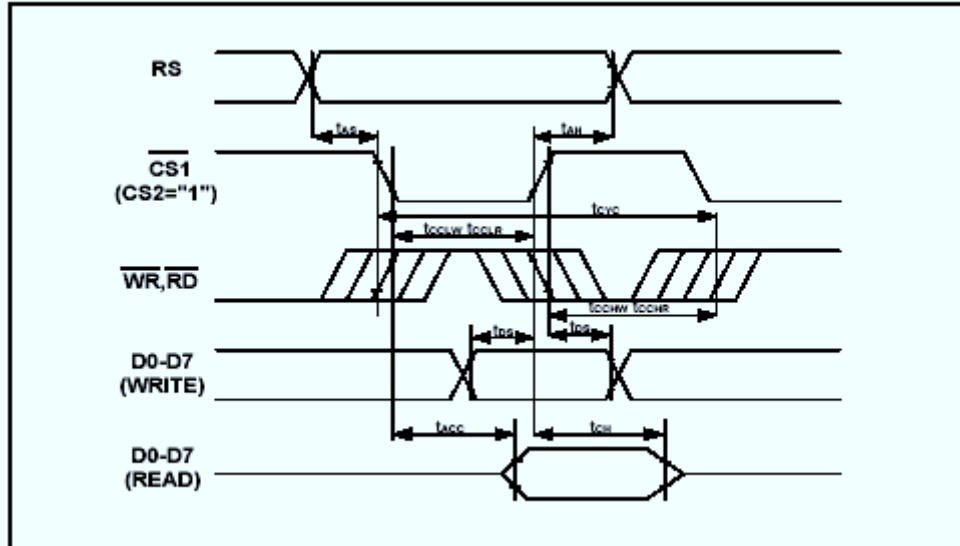


Figure 12-1 8080 CPU system waveforms

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$T_{AH}$	Address hold time	17			ns	
$T_{AS}$	Address setup time	13			ns	
$T_{CYC}$	System cycle time	400			ns	
$T_{CCLW}$	Control L pulse width (WR)	55			ns	
$T_{CCLR}$	Control L pulse width (RD)	125			ns	
$T_{CCHW}$	Control H pulse width (WR)	180			ns	
$T_{CCHR}$	Control H pulse width (RD)	130			ns	
$T_{DS}$	Data setup time	35			ns	
$T_{DH}$	data hold time	13			ns	
$T_{ACC}$	RD# access time			125	ns	$C_L=100\text{pF}$
$T_{CH}$	Output disable time	10		90	ns	$C_L=100\text{pF}$

## 12.2 6800 CPU System Buses

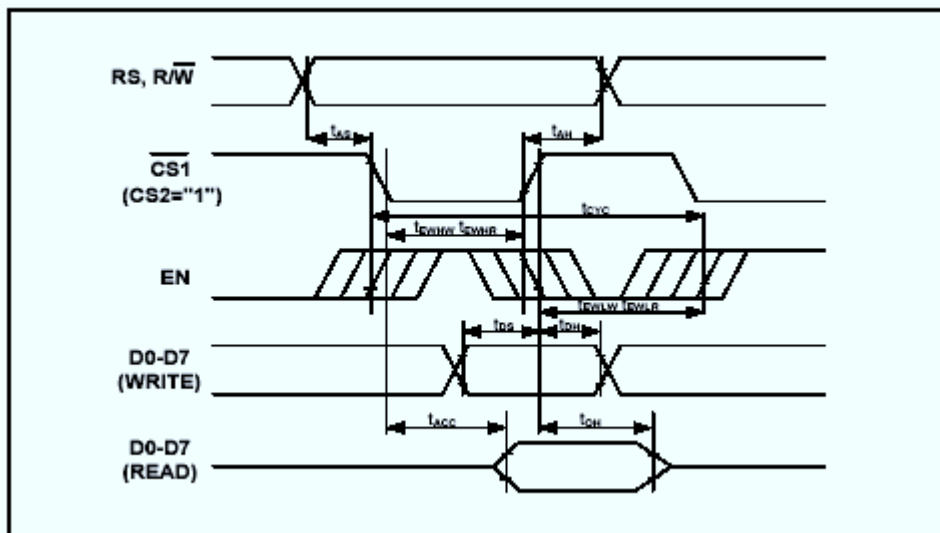


Figure 12-2 6800 CPU system waveforms

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$T_{CYC}$	System cycle time	400			ns	
$T_{AS}$	Address setup time	13			ns	
$T_{CYC}$	Address hold time	17			ns	
$T_{AH}$	Data setup time	35			ns	
$T_{DS}$	Data hold time	13			ns	
$T_{DH}$	Output disable time	10		90	ns	$C_L=100pF$
$T_{QH}$	Access time			125	ns	$C_L=100pF$
$T_{ACC}$	Enable	125			ns	
$T_{EWLR}$	Low pulse width	55			ns	
$T_{EWHR}$	Enable	125			ns	
$T_{EWHW}$	High pulse width	180			ns	

## 12.3 RA8802 External ROM Interface

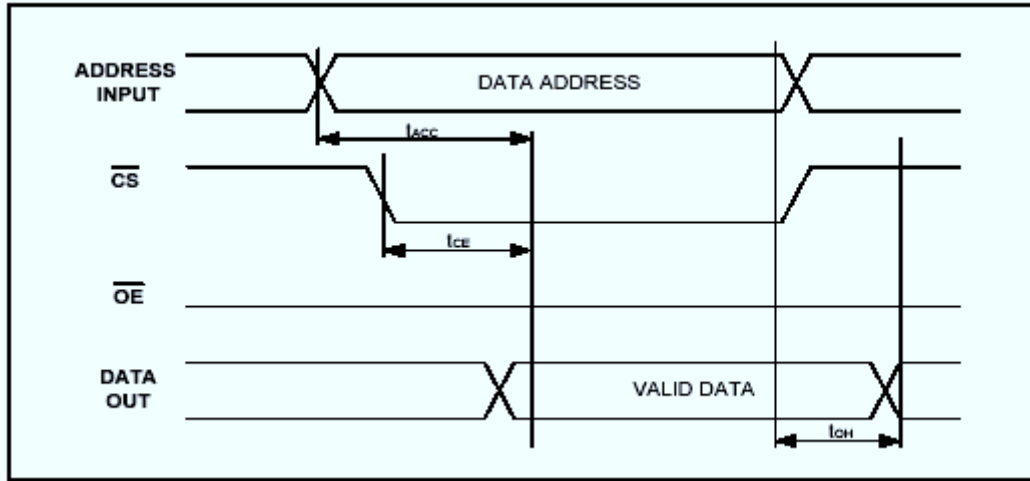


Figure 12-3 RA8802 External ROM Interface waveforms

SYMBLE	PARAMETER	MX27C8000-15	MIN.	MAX.	UNIT
$t_{acc}$	Address to Output Delay			150	ns
$t_{cs}$	Chip Select to Output Delay			150	ns
$t_{oh}$	Output Hold from Address		0		ns

## 13. Microprocessor Interface

### 13.1 8080-series microprocessors (4/8-bit)

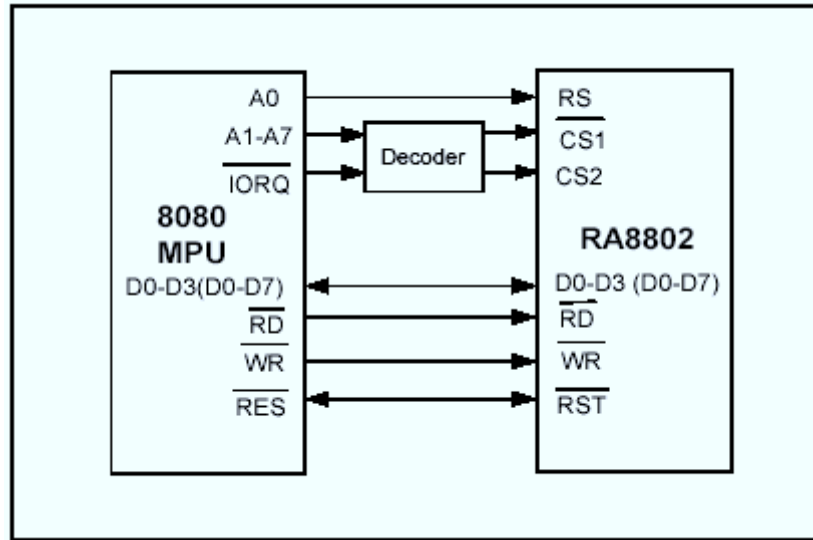


Figure 13-1 8080 (4/8-bit) CPU with RA8802 connection

### 13.2 6800-series microprocessors (4/8-bit)

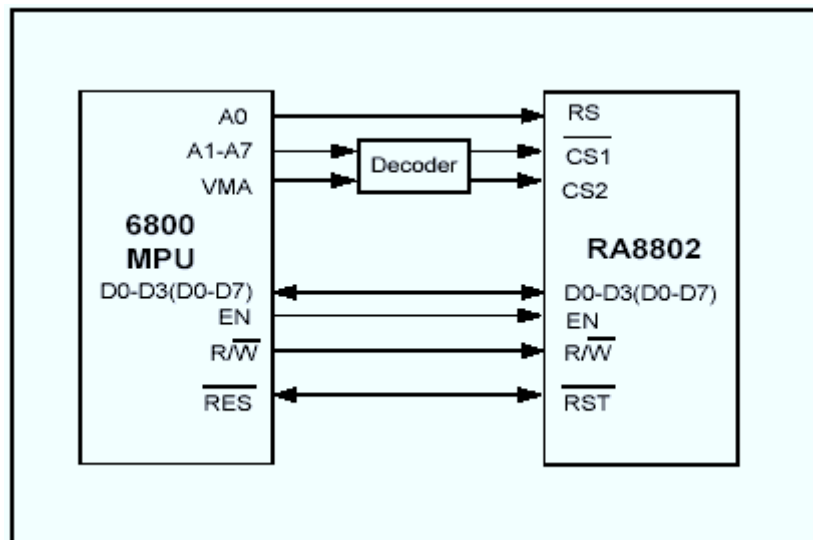
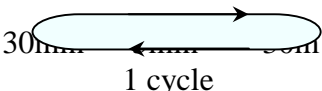


Figure 13-2 6800 (4/8-bit) CPU with RA8802 connection

## 14. Reliability

### Content of Reliability Test (wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	— —
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C, 90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60°C, 90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20°C    25°C    70°C  	-20°C/70°C 10 cycles	— —
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 15mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	— —

**Note1:** No dew condensation to be observed.

**Note2:** The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

**Note3:** Vibration test will be conducted to the product itself without putting it in a container.

## **15.Backlight Information**

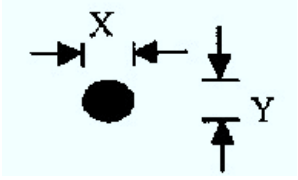
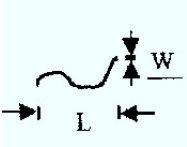
### **Specification**

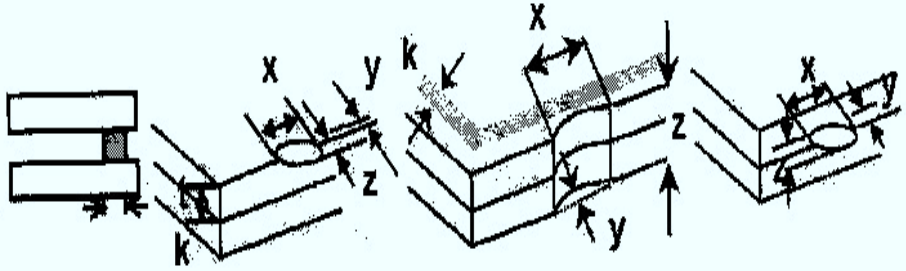
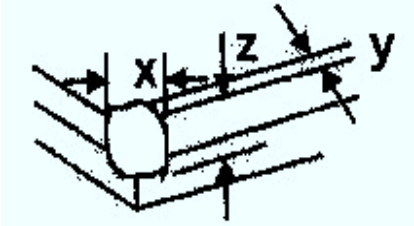
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	I <sub>LED</sub>	144	180	270	mA	V=3.5V
Supply Voltage	V	3.4	3.5	3.6	V	
Reverse Voltage	V <sub>R</sub>	—	—	8	V	
Luminous Intensity	I <sub>V</sub>	—	220	—	CD/M <sup>2</sup>	I <sub>LED</sub> =180mA
Wave Length	λ <sub>p</sub>				nm	I <sub>LED</sub> =180mA
Life Time		—	50000	—	Hr.	I <sub>LED</sub> =180mA
Color	White					

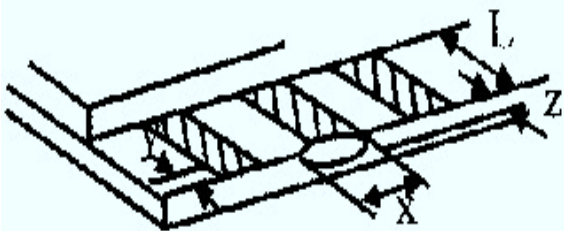
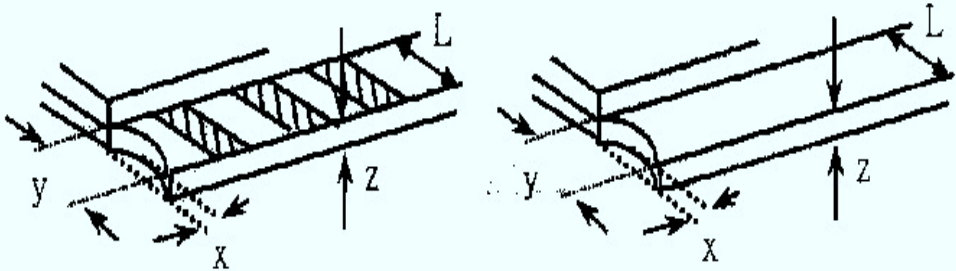
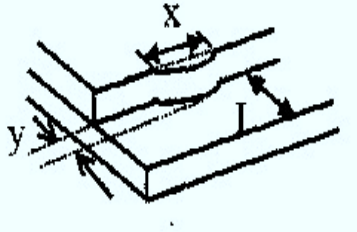
**Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).**

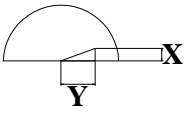


## 16. Inspection specification

NO	Item	Criterion	AQL												
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65												
02	Black or white spots on LCD (display only)	2.1 White and black spots on display $\leq 0.25\text{mm}$ , no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5												
03	LCD black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing $\Phi = (x + y) / 2$  <table border="1" data-bbox="858 1025 1337 1243"> <thead> <tr> <th>SIZE</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.10</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.20</math></td> <td>2</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.25</math></td> <td>1</td> </tr> <tr> <td><math>0.25 &lt; \Phi</math></td> <td>0</td> </tr> </tbody> </table>	SIZE	Acceptable Q TY	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0	2.5		
		SIZE	Acceptable Q TY												
$\Phi \leq 0.10$	Accept no dense														
$0.10 < \Phi \leq 0.20$	2														
$0.20 < \Phi \leq 0.25$	1														
$0.25 < \Phi$	0														
3.2 Line type : (As following drawing)  <table border="1" data-bbox="694 1355 1337 1568"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>W \leq 0.02</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>L \leq 3.0</math></td> <td><math>0.02 &lt; W \leq 0.03</math></td> <td rowspan="2">2</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.03 &lt; W \leq 0.05</math></td> </tr> <tr> <td>---</td> <td><math>0.05 &lt; W</math></td> <td>As round type</td> </tr> </tbody> </table>	Length	Width	Acceptable Q TY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	---	$0.05 < W$	As round type	2.5
Length	Width	Acceptable Q TY													
---	$W \leq 0.02$	Accept no dense													
$L \leq 3.0$	$0.02 < W \leq 0.03$	2													
$L \leq 2.5$	$0.03 < W \leq 0.05$														
---	$0.05 < W$	As round type													
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction. <table border="1" data-bbox="826 1612 1337 1870"> <thead> <tr> <th>Size <math>\Phi</math></th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.20</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.50</math></td> <td>3</td> </tr> <tr> <td><math>0.50 &lt; \Phi \leq 1.00</math></td> <td>2</td> </tr> <tr> <td><math>1.00 &lt; \Phi</math></td> <td>0</td> </tr> <tr> <td>Total Q TY</td> <td>3</td> </tr> </tbody> </table>	Size $\Phi$	Acceptable Q TY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total Q TY	3	2.5
Size $\Phi$	Acceptable Q TY														
$\Phi \leq 0.20$	Accept no dense														
$0.20 < \Phi \leq 0.50$	3														
$0.50 < \Phi \leq 1.00$	2														
$1.00 < \Phi$	0														
Total Q TY	3														

NO	Item	Criterion	AQL																		
05	Scratches	Follow NO.3 LCD black spots, white spots, contamination																			
06	Chipped glass	<p>Symbols Define:                      x: Chip length      y: Chip width      z: Chip thickness                      k: Seal width      t: Glass thickness      a: LCD side length                      L: Electrode pad length:</p> <p>6.1 General glass chip :                      6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="427 987 1337 1115"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td><math>Z \leq 1/2t</math></td> <td>Not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> <tr> <td><math>1/2t &lt; z \leq 2t</math></td> <td>Not exceed 1/3k</td> <td><math>x \leq 1/8a</math></td> </tr> </table> <p>⊙If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p>  <table border="1" data-bbox="427 1505 1337 1632"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td><math>Z \leq 1/2t</math></td> <td>Not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> <tr> <td><math>1/2t &lt; z \leq 2t</math></td> <td>Not exceed 1/3k</td> <td><math>x \leq 1/8a</math></td> </tr> </table> <p>⊙If there are 2 or more chips, x is the total length of each chip.</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			

NO	Item	Criterion	AQL						
06	Glass crack	<p>Symbols :</p> <p>x: Chip length      y: Chip width      z: Chip thickness</p> <p>k: Seal width      t: Glass thickness      a: LCD side length</p> <p>L: Electrode pad length</p> <p>6.2 Protrusion over terminal :</p> <p>6.2.1 Chip on electrode pad :</p>	2.5						
		 <table border="1" data-bbox="336 882 1249 969"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td><math>y \leq 0.5\text{mm}</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </table>		y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$
		y: Chip width		x: Chip length	z: Chip thickness				
		$y \leq 0.5\text{mm}$		$x \leq 1/8a$	$0 < z \leq t$				
<p>6.2.2 Non-conductive portion:</p>  <table border="1" data-bbox="408 1301 1249 1388"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td><math>y \leq L</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$			
y: Chip width	x: Chip length	z: Chip thickness							
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$							
<p>⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.</p> <p>6.2.3 Substrate protuberance and internal crack.</p>  <table border="1" data-bbox="746 1610 1254 1697"> <tr> <td>y: width</td> <td>x: length</td> </tr> <tr> <td><math>y \leq 1/3L</math></td> <td><math>x \leq a</math></td> </tr> </table>	y: width	x: length	$y \leq 1/3L$	$x \leq a$					
y: width	x: length								
$y \leq 1/3L$	$x \leq a$								

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB  $X * Y \leq 2\text{mm}^2$	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		12.2 No cracks on interface pin (OLB) of TCP.	0.65
		12.3 No contamination, solder residue or solder balls on product.	2.5
		12.4 The IC on the TCP may not be damaged, circuits.	2.5
		12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.	2.5
		12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	2.5
		12.7 Sealant on top of the ITO circuit has not hardened.	2.5
		12.8 Pin type must match type in specification sheet.	0.65
		12.9 LCD pin loose or missing pins.	0.65
		12.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		12.11 Product dimension and structure must conform to product specification sheet.	0.65

**LCM Sample Estimate Feedback Sheet**

Module Number : \_\_\_\_\_

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**1、Panel Specification :**

1. Panel Type :  Pass  NG , \_\_\_\_\_
2. View Direction :  Pass  NG , \_\_\_\_\_
3. Numbers of Dots :  Pass  NG , \_\_\_\_\_
4. View Area :  Pass  NG , \_\_\_\_\_
5. Active Area :  Pass  NG , \_\_\_\_\_
6. Operating Temperature :  Pass  NG , \_\_\_\_\_
7. Storage Temperature :  Pass  NG , \_\_\_\_\_
8. Others : \_\_\_\_\_

**2、Mechanical Specification :**

1. PCB Size :  Pass  NG , \_\_\_\_\_
2. Frame Size :  Pass  NG , \_\_\_\_\_
3. Material of Frame :  Pass  NG , \_\_\_\_\_
4. Connector Position :  Pass  NG , \_\_\_\_\_
5. Fix Hole Position : A  Pass  NG , \_\_\_\_\_
6. Backlight Position :  Pass  NG , \_\_\_\_\_
7. Thickness of PCB :  Pass  NG , \_\_\_\_\_
8. Height of Frame to PCB :  Pass  NG , \_\_\_\_\_
9. Height of Module :  Pass  NG , \_\_\_\_\_
10. Others :  Pass  NG , \_\_\_\_\_

**3、Relative Hole Size :**

1. Pitch of Connector :  Pass  NG , \_\_\_\_\_
2. Hole size of Connector :  Pass  NG , \_\_\_\_\_
3. Mounting Hole size :  Pass  NG , \_\_\_\_\_
4. Mounting Hole Type :  Pass  NG , \_\_\_\_\_
5. Others :  Pass  NG , \_\_\_\_\_

**4、Backlight Specification :**

1. B/L Type :  Pass  NG , \_\_\_\_\_
2. B/L Color :  Pass  NG , \_\_\_\_\_

- 3. B/L Driving Voltage (Reference for LED Type) :  Pass  NG ,\_\_\_\_\_
- 4. B/L Driving Current :  Pass  NG ,\_\_\_\_\_
- 5. Brightness of B/L :  Pass  NG ,\_\_\_\_\_
- 6. B/L Solder Method :  Pass  NG ,\_\_\_\_\_
- 7. Others :  Pass  NG ,\_\_\_\_\_

>> Go to page 2 <<

Module Number : \_\_\_\_\_

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**5、Electronic Characteristics of Module :**

- 1. Input Voltage :  Pass  NG ,\_\_\_\_\_
- 2. Supply Current :  Pass  NG ,\_\_\_\_\_
- 3. Driving Voltage for LCD :  Pass  NG ,\_\_\_\_\_
- 4. Contrast for LCD :  Pass  NG ,\_\_\_\_\_
- 5. B/L Driving Method :  Pass  NG ,\_\_\_\_\_
- 6. Negative Voltage Output :  Pass  NG ,\_\_\_\_\_
- 7. Interface Function :  Pass  NG ,\_\_\_\_\_
- 8. LCD Uniformity :  Pass  NG ,\_\_\_\_\_
- 9. ESD test :  Pass  NG ,\_\_\_\_\_
- 10. Others :  Pass  NG ,\_\_\_\_\_

**6、Summary :**

Sales signature : \_\_\_\_\_

Customer Signature : \_\_\_\_\_

Date :     /     /     \_\_\_\_\_