



中显液晶  
技术资料



## 中显控制器使用说明书

2009年3月15日

北京市海淀区中关村大街32号和盛大厦811室  
电话：(86)-010-52926620 传真：(86)-010-52926621  
企业网站：<http://www.zxlcd.com>

**INTRODUCTION**

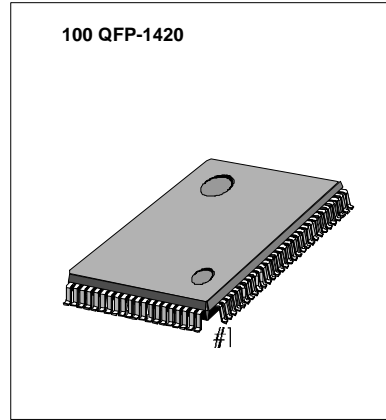
The KS0107B is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display system. This device provides 64 shift register and 64 output driver. It generates the timing signal to control the KS0108B segment driver. The KS0107B is fabricated by low power CMOS high voltage process technology and compose of the liquid crystal display system in combination with the KS0108B segment driver.

**FEATURES**

- Dot matrix LCD common driver with 64 channel output.
- 64 bits shift register of internal LCD driver circuit.
- Internal timing generator circuit for dynamic display.
- Selectable master/slave mode.
  
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: + 5V ±10%
- LCD driving voltage: 8V~17V( $V_{DD}-V_{EE}$ )
- Interface

Driver		controller
COMMON	SEGMENT	
Other KS0107B	KS0108B	MPU

- High voltage CMOS process.
- 100QFP and bare chip available.



**BLOCK DIAGRAM**

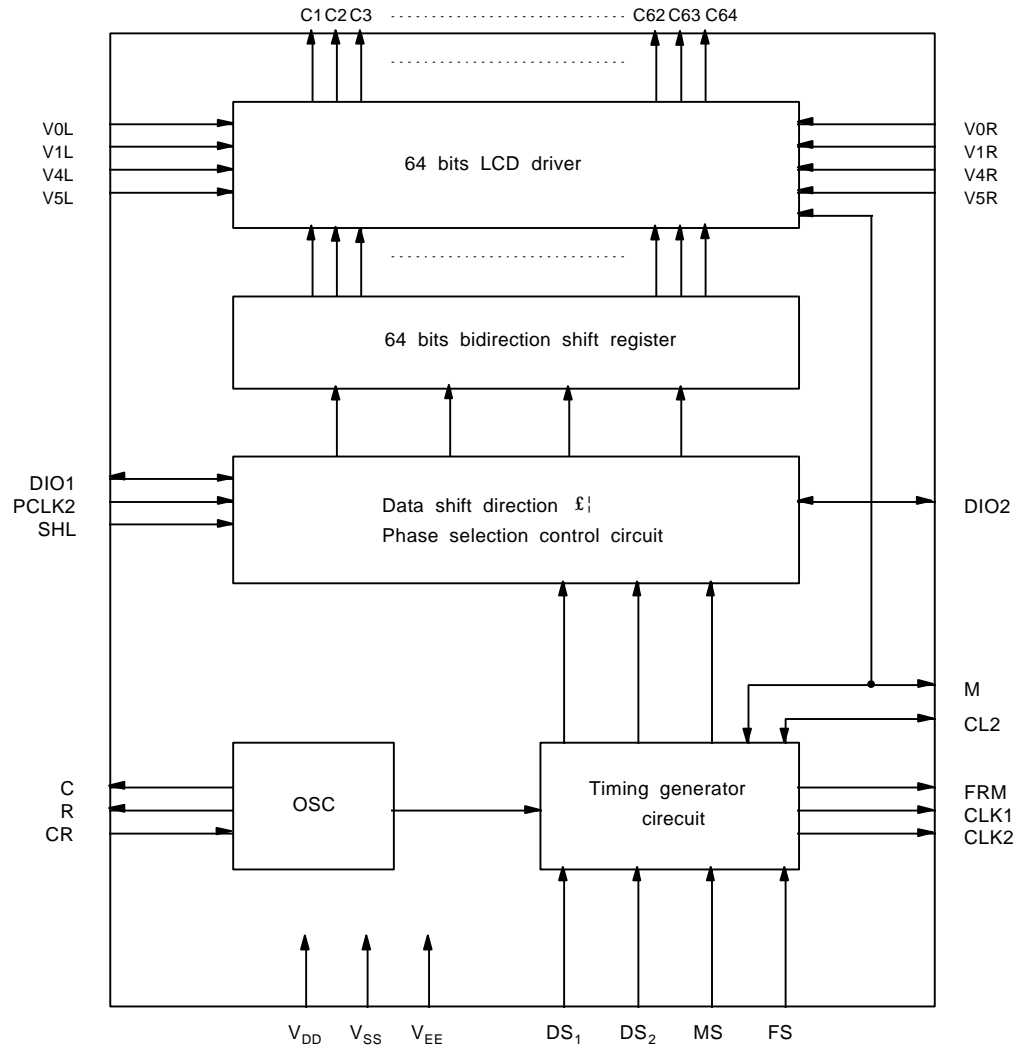


Fig. 1. KS0107B Functional block diagram

PIN CONFIGURATION

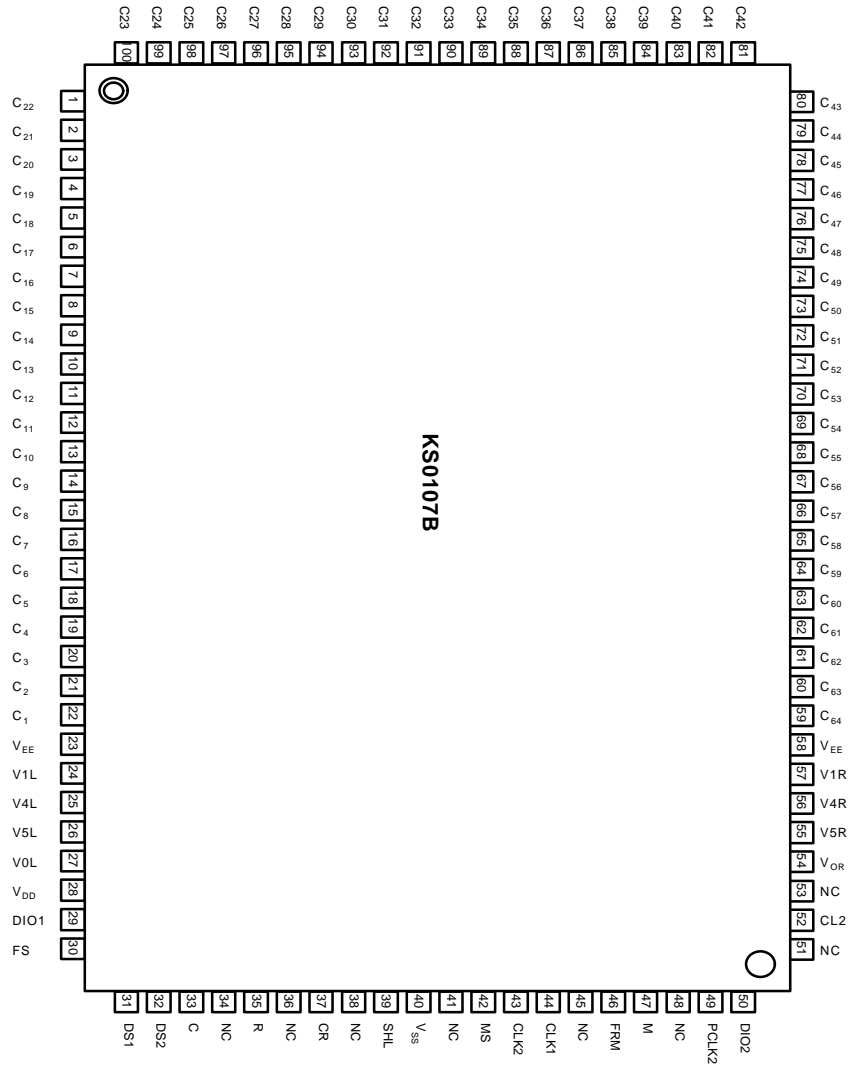
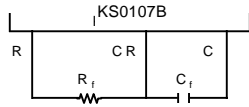
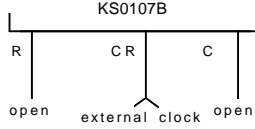
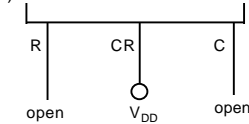


Fig. 2. 100 QFP Top View

PIN DESCRIPTION

PIN(NO)	SYMBOL	INPUT/OUTPUT	DESCRIPTION															
28 40 23,58	V <sub>DD</sub> V <sub>SS</sub> V <sub>EE</sub>	Power	For internal logic circuit (+5V±10%) GND (0V) For LCD driver circuit															
27, 54 24, 57 25, 56 26, 55	V0L, V0R V1L, V1R V4L, V4R V5L, V5R	Power	Bias supply voltage terminals to drive LCD. <table border="1" style="margin-left: 20px;"> <tr> <td>Select Level</td> <td>Non-Select Level</td> </tr> <tr> <td>V0L(R), V5L(R)</td> <td>V1L(R), V4L(R)</td> </tr> </table> <p>V0L and V0R is connected by the same voltage.</p>	Select Level	Non-Select Level	V0L(R), V5L(R)	V1L(R), V4L(R)											
Select Level	Non-Select Level																	
V0L(R), V5L(R)	V1L(R), V4L(R)																	
42	MS	Input	Selection of master/slave mode i) Master mode (MS=1) DIO1, DIO2, CL2 and M is output state. ii) Slave mode (MS=0) SHL=1 → DIO1 is input state(DIO2 is output state) SHL=0 → DIO2 is input state(DIO1 is output state) CL2 and M is input state.															
39	SHL	Input	Selection of data shift direction. <table border="1" style="margin-left: 20px;"> <tr> <td>SHL</td> <td>Data shift direction</td> </tr> <tr> <td>H</td> <td>DIO1→C1→...→C64→DIO2</td> </tr> <tr> <td>L</td> <td>DIO2→C64→...→C1→DIO1</td> </tr> </table>	SHL	Data shift direction	H	DIO1→C1→...→C64→DIO2	L	DIO2→C64→...→C1→DIO1									
SHL	Data shift direction																	
H	DIO1→C1→...→C64→DIO2																	
L	DIO2→C64→...→C1→DIO1																	
49	PCLK2	Input	Selection of shift clock (CL2) phase. <table border="1" style="margin-left: 20px;"> <tr> <td>PCLK2</td> <td>shift clock(CL2) phase</td> </tr> <tr> <td>H</td> <td>data shift at the rising edge of CL2</td> </tr> <tr> <td>L</td> <td>data shift at the falling edge of CL2</td> </tr> </table>	PCLK2	shift clock(CL2) phase	H	data shift at the rising edge of CL2	L	data shift at the falling edge of CL2									
PCLK2	shift clock(CL2) phase																	
H	data shift at the rising edge of CL2																	
L	data shift at the falling edge of CL2																	
30	FS	Input	Selection of oscillation frequency. i) Master mode When the freme frequency is 70Hz, the oscillation frequency should be fosc=430KHz at FS=1 (V <sub>DD</sub> ) fosc=215KHz at FS=0 (V <sub>SS</sub> ) ii) Slave mode Connect to V <sub>DD</sub> .															
31 32	DS1, DS2	Input	Selection of display duty. i) Master mode <table border="1" style="margin-left: 20px;"> <tr> <td>DS1</td> <td>DS2</td> <td>Duty</td> </tr> <tr> <td>L</td> <td>L</td> <td>1/48</td> </tr> <tr> <td>L</td> <td>H</td> <td>1/64</td> </tr> <tr> <td>H</td> <td>L</td> <td>1/96</td> </tr> <tr> <td>H</td> <td>H</td> <td>1/128</td> </tr> </table> ii) Slave mode : Connect to V <sub>DD</sub> .	DS1	DS2	Duty	L	L	1/48	L	H	1/64	H	L	1/96	H	H	1/128
DS1	DS2	Duty																
L	L	1/48																
L	H	1/64																
H	L	1/96																
H	H	1/128																

PIN DESCRIPTION (continued)

PIN(NO)	SYMBOL	INPUT/OUTPUT	DESCRIPTION																		
33 35 37	C R CR		<p>RC Oscillator</p> <p>i) Master mode</p>   <p>ii) Slave mode</p> 																		
44, 43	CLK1, CLK2	Output	<p>Operating clock output for the KS0108B</p> <p>i) Master mod Connection to CLK1 and CLK2 of the KS0108B</p> <p>ii) Slave mode Open</p>																		
46	FRM	Output	<p>Synchronous frame signal.</p> <p>i) Master mode Connection to FRM of the KS0108B</p> <p>ii) Slave mode Open</p>																		
47	M	Input/Output	<p>Alternating signal input for LCD driving.</p> <p>i) Master mode: output state Connection to M of the KS0108B</p> <p>ii) Slave mode: input state Connection to the controller</p>																		
52	CL2	Input/Output	<p>Data shift clock</p> <p>i) Master mode: output state Connection to CL of the KS0108B</p> <p>ii) Slave mode: input state Connection to shift clock terminal of the controller.</p>																		
29 50	DIO1 DIO2	Input/Output	<p>Data input/output pin of internal shift register.</p> <table border="1" data-bbox="662 1160 1093 1288"> <thead> <tr> <th>MS</th> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Output</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	MS	SHL	DIO1	DIO2	H	H	Output	Output	L	Output	Output	L	H	Input	Output	L	Output	Input
MS	SHL	DIO1	DIO2																		
H	H	Output	Output																		
	L	Output	Output																		
L	H	Input	Output																		
	L	Output	Input																		
22-1 100-59	C1~C64	Output	<p>Common signal output for LCD driving.</p> <table border="1" data-bbox="662 1355 1093 1478"> <thead> <tr> <th>DATA</th> <th>M</th> <th>OUT</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>V<sub>1</sub></td> </tr> <tr> <td>L</td> <td>H</td> <td>V<sub>4</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>V<sub>5</sub></td> </tr> <tr> <td>H</td> <td>H</td> <td>V<sub>0</sub></td> </tr> </tbody> </table>	DATA	M	OUT	L	L	V <sub>1</sub>	L	H	V <sub>4</sub>	H	L	V <sub>5</sub>	H	H	V <sub>0</sub>			
DATA	M	OUT																			
L	L	V <sub>1</sub>																			
L	H	V <sub>4</sub>																			
H	L	V <sub>5</sub>																			
H	H	V <sub>0</sub>																			
34,36,38,41 45,48,51,53	NC		No Connection																		

## MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	$V_{DD}$	-0.3~+7.0	V	*1
Supply Voltage	$V_{EE}$	$V_{DD}-19.0-V_{DD}+0.3$	V	*4
Driver Supply Voltage	$V_B$	-0.3~ $V_{DD}+0.3$	V	*1,2
	$V_{LCD}$	$V_{EE}-0.3-V_{DD}+0.3$	V	*3,4
Operating Temperature	$T_{OPR}$	-30~+85	°C	-
Storage Temperature	$T_{STG}$	-55~+125	°C	-

\*1. Based on  $V_{SS}=0V$

\*2. Applies to input terminals and I/O terminals at high impedance.  
(Except  $V_{0L(R)}$ ,  $V_{1L(R)}$ ,  $V_{4L(R)}$  and  $V_{5L(R)}$ )

\*3. Applies to  $V_{0L(R)}$ ,  $V_{1L(R)}$ ,  $V_{4L(R)}$  and  $V_{5L(R)}$ .

\*4. Voltage level:  $V_{DD} \geq V_{0L} = V_{0R} \geq V_{1L} = V_{1R} \geq V_{4L} = V_{4R} \geq V_{5L} = V_{5R} \geq V_{EE}$ .

## ELECTRICAL CHARACTERISTICS

DC Characteristics ( $V_{DD}=+5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $|V_{DD}-V_{EE}|=8\sim 17V$ ,  $T_a=-30 \sim +85^\circ C$ )

Characteristic	Symbol	condition	Min	Typ	Max	Unit	Note
Input Voltage	High	-	$0.7V_{DD}$	-	$V_{DD}$	V	*1
	Low		$V_{SS}$	-	$0.3V_{DD}$		
Output Voltage	Hogh	$I_{OH}=-0.4mA$	$V_{DD}-0.4$	-	-	V	*2
	Low	$I_{OL}=0.4mA$	-	-	0.4		
Input Leakage Current	$I_{LKG}$	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	$\mu A$	*1
OSC Frequency	$f_{OSC}$	$R_f=47K\Omega \pm 2\%$ $C_f=20pf \pm 5\%$	315	450	585	KHz	
On Resistance (Vdiv-Ci)	$R_{ON}$	$V_{DD}-V_{EE}=17V$ Load current $\pm 150\mu A$	-	-	1.5	$K\Omega$	
Operating Current	$I_{DD1}$	Master mode 1/128 Duty	-	-	1.0	$mA$	*3
	$I_{DD2}$	Slave mode 1/128 Duty	-	-	200		$\mu A$
Supply Current	$I_{EE}$	Master mode 1/128 Duty	-	-	100		*5
Operating Frequency	$f_{op1}$	Master mode External clock	50	-	600	KHz	
	$f_{op2}$	Slave mode	0.5	-	1500		

\*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.

\*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.

\*3. This value is specified about current flowing through  $V_{SS}$ .

Internal oscillation circuit:  $R_f=47k\Omega$ ,  $C_f=20pF$

Each terminals of DS1, DS2, FS, SHL and MS is connected to  $V_{DD}$  and out is no load.

\*4. This value is specified about current flowing through  $V_{SS}$ .

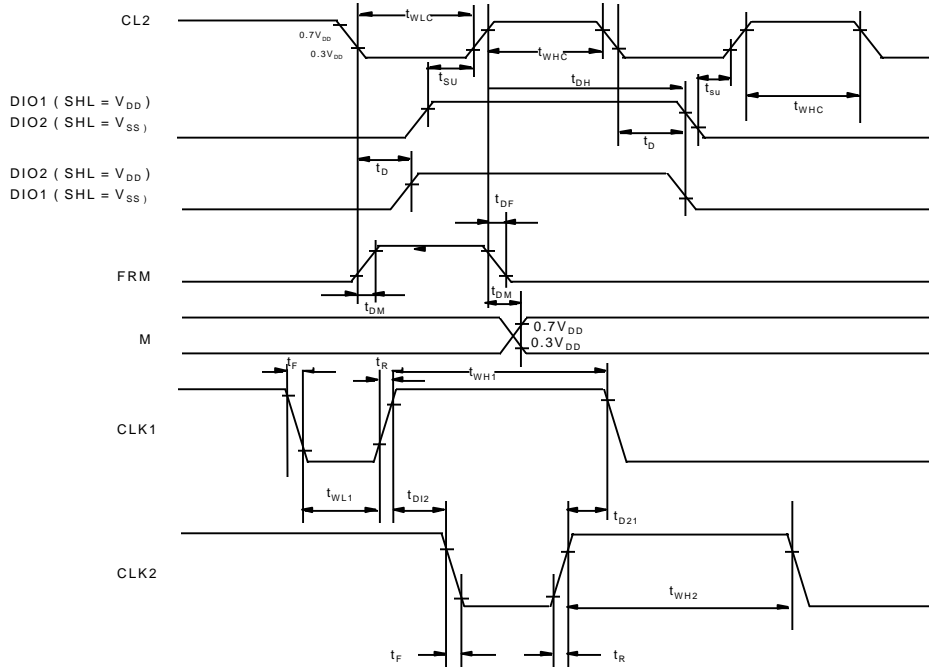
Each terminals is DS1, DS2, FS, SHL, PCLK2 and CR is connected to  $V_{DD}$ , MS is connected to  $V_{SS}$  and CL2, M, DIO1 is external clock.

\*5. This value is specified about current flowing through  $V_{EE}$ .

Don't connect to  $V_{LCD}$  (V1~V5).

**AC Characteristics** (VDD=5V±10%, Ta=-30°C~+85°C)

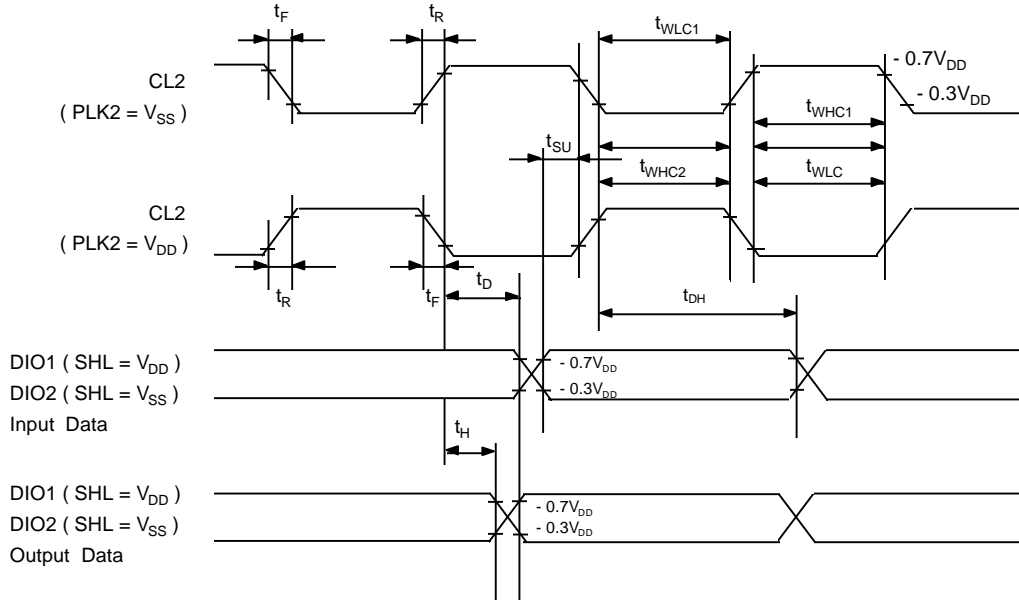
(1) Master mode (MS=VDD, PCLK2=VDD, Cf=20pF, Rf=47KΩ)



Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	$t_{SU}$	20	-	-	μs
Data Hold Time	$t_{DH}$	40	-	-	
Data Delay Time	$t_D$	5	-	-	
FRM Delay Time	$t_{DF}$	-2	-	2	
M Delay Time	$t_{DM}$	-2	-	2	
CL2 Low Level Width	$t_{WLC}$	35	-	-	
CL2 High Level Width	$t_{WHC}$	35	-	-	ns
CLK1 Low Level Width	$t_{WL1}$	700	-	-	
CLK2 Low Level Width	$t_{WL2}$	700	-	-	
CLK1 High Level Width	$t_{WH1}$	2100	-	-	
CLK2 High Level Width	$t_{WH2}$	2100	-	-	
CLK1-CLK2 Phase Difference	$t_{D12}$	700	-	-	
CLK2-CLK1 Phase Difference	$t_{D21}$	700	-	-	
CLK1, CLK2 Rise/Fall Time	$t_R/t_F$	-	-	150	

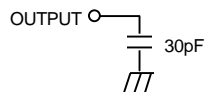


(2) Slave mode (MS=V<sub>SS</sub>)



Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t <sub>WLC1</sub>	450	-	-	ns	PCLK2=V <sub>SS</sub>
CL2 High Level Width	t <sub>WHC1</sub>	150	-	-	ns	PCLK2=V <sub>SS</sub>
CL2 Low Level Width	t <sub>WLC2</sub>	150	-	-	ns	PCLK2=V <sub>DD</sub>
CL2 High Level Width	t <sub>WHL</sub>	450	-	-	ns	PCLK2=V <sub>DD</sub>
Data Setup Time	t <sub>SU</sub>	100	-	-	ns	
Data Hold Time	t <sub>DH</sub>	100	-	-	ns	
Data Delay Time	t <sub>D</sub>	-	-	200	ns	*1
Output Data Hold Time	t <sub>H</sub>	10	-	-	ns	
CL2 Rise/Fall Time	t <sub>R</sub> /t <sub>F</sub>	-	-	30	ns	

\*1; Connect load CL=30pF



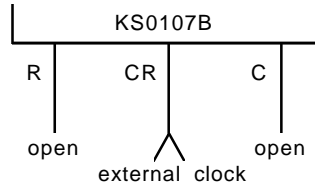
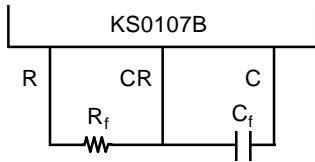
**FUNCTIONAL DESCRIPTION**

**1.RC Oscillator**

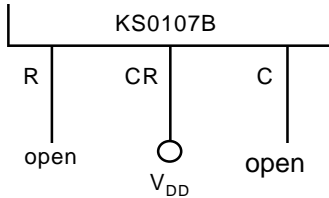
The RC Oscillator generates CL2, M,FRM, of the KS0107B and CLK1, CLK2 of the KS0108B by the oscillation resistor R and capacitor C.

When selecting the master/slave, oscillation circuit is as following:

1) Master Mode



2) Slave Mode



**2. Timing Generation Circuit**

It generates CL2, M, FRM, CLK1, and CLK2 by the frequency from oscillation circuit.

1) Selection of Master/Slave (M/S)

When M/S, is "H", it generates CL2, M, FRM, CLK1, and CLK2 internally. When M/S is "L", it operates by receiving M, CL2 from master device.

2) Frequency Selection (FS)

To adjust FRM by 70Hz, the oscillation frequency should be as following:

FS	Oscillation Frequency
H	f <sub>OSC</sub> =430KHz
L	f <sub>OSC</sub> =215KHz

In the slave mode, it is connected to V<sub>DD</sub>.

3) Duty Selection (DS1, DS2)

It provides various duty selection according to DS1, DS2.

DS1	DS2	DUTY
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

**3. Data Shift & Phase Select Control**

## 1) Phase Selection

It is a circuit to shift data on synchronization or rising edge or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

## 2) Data Shift Direction Selection

When M/S is connected to  $V_{DD}$ , DIO1 and DIO2 terminal is only output.

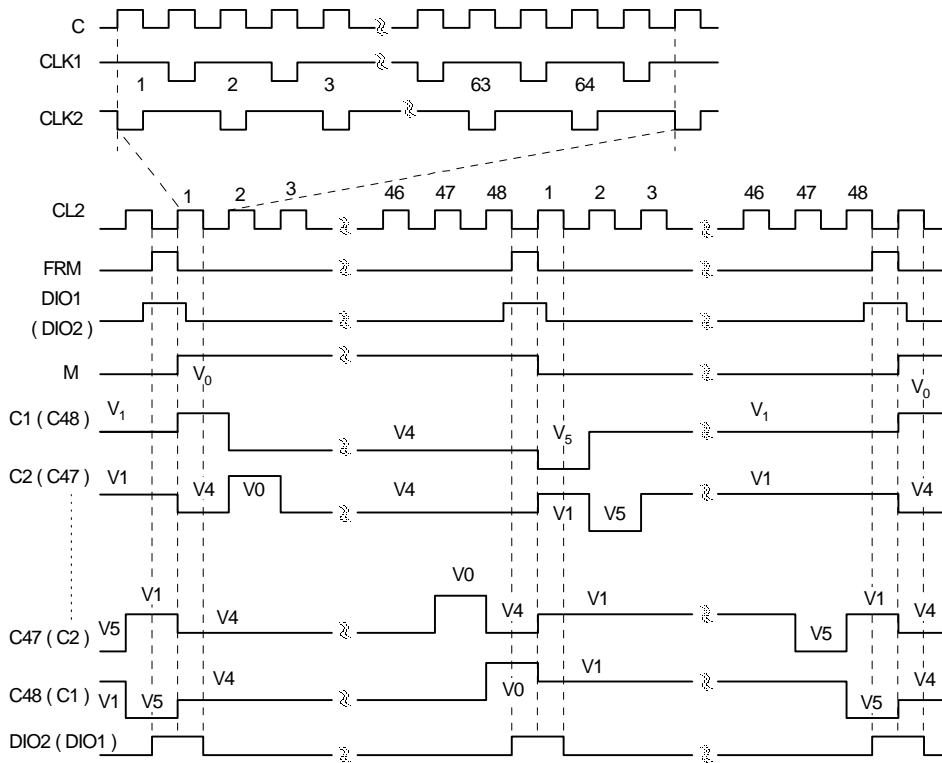
When M/S is connected to  $V_{SS}$ , it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1→C64
	L	Output	Output	C64→C1
L	H	Input	Output	DIO1→C1→C64→DIO2
	L	Output	Input	DIO2→C64→C1→DIO1

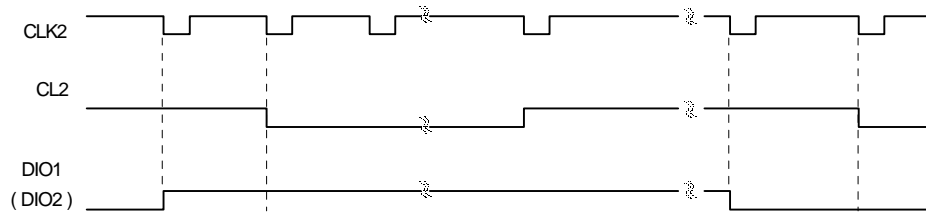
**TIMING DIAGRAM**

(1) 1/48 duty timing (Master mode)

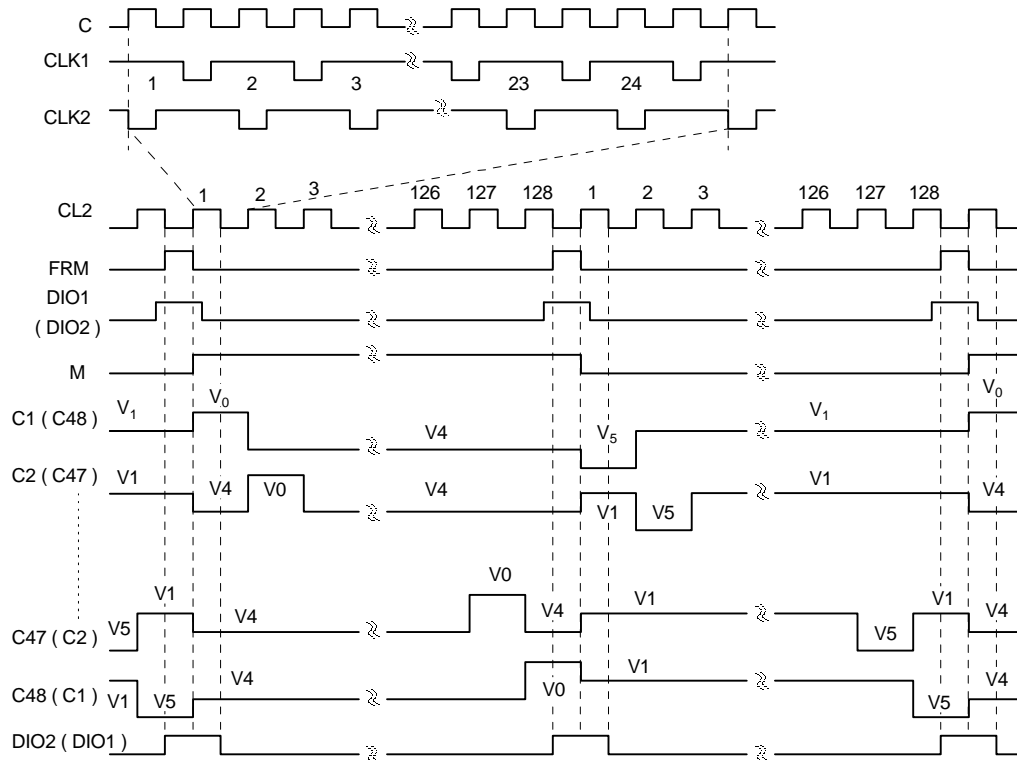
Condition: DS1=L, DS=L, SHL=H(L), PCLK2=H



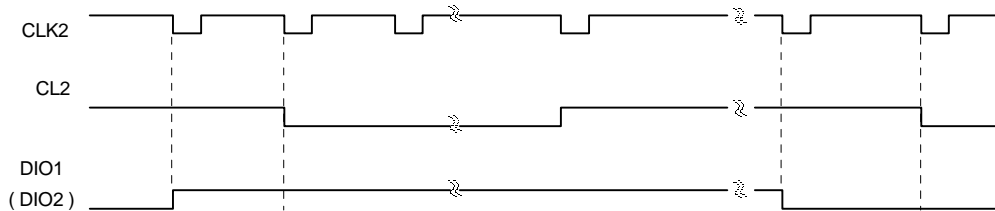
- relation of CL2 and DIO1 (DIO2)



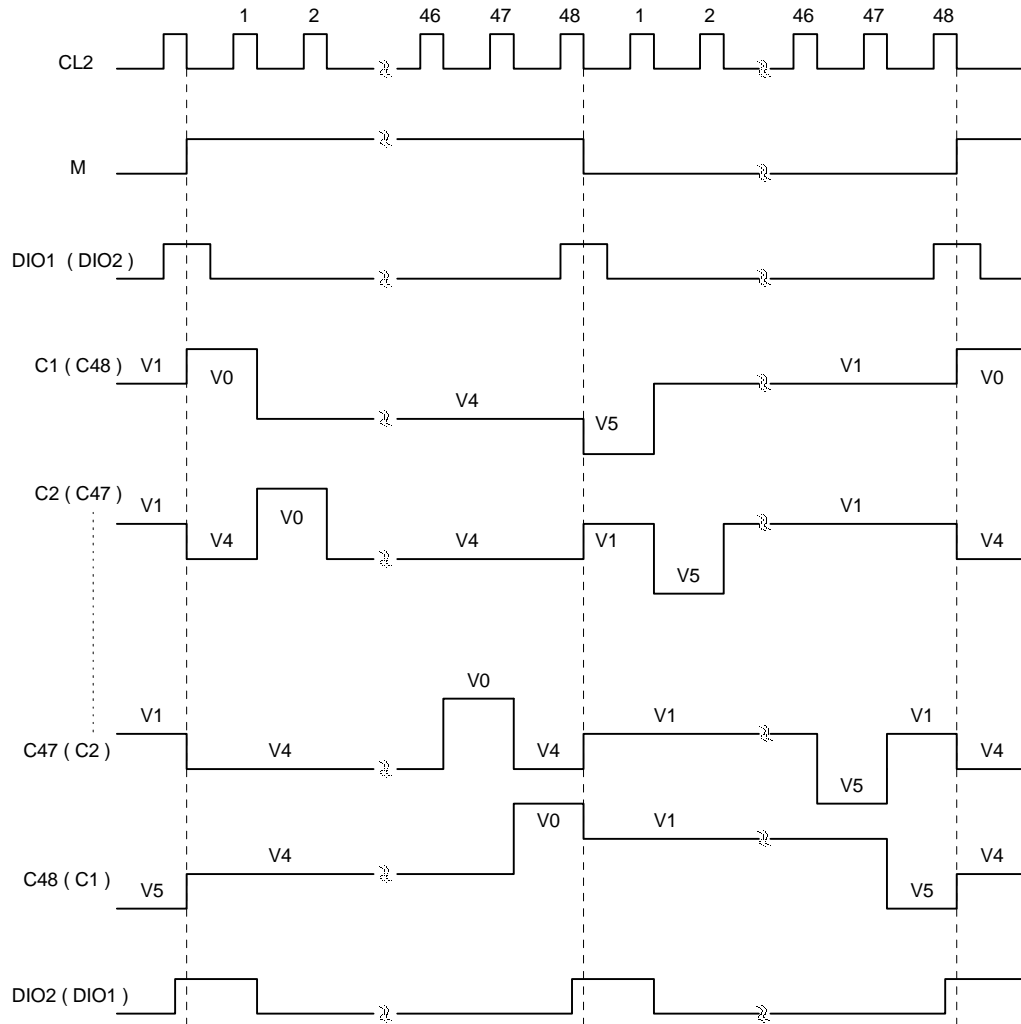
(2) 1/128 duty timing (Master mode)  
 - Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H



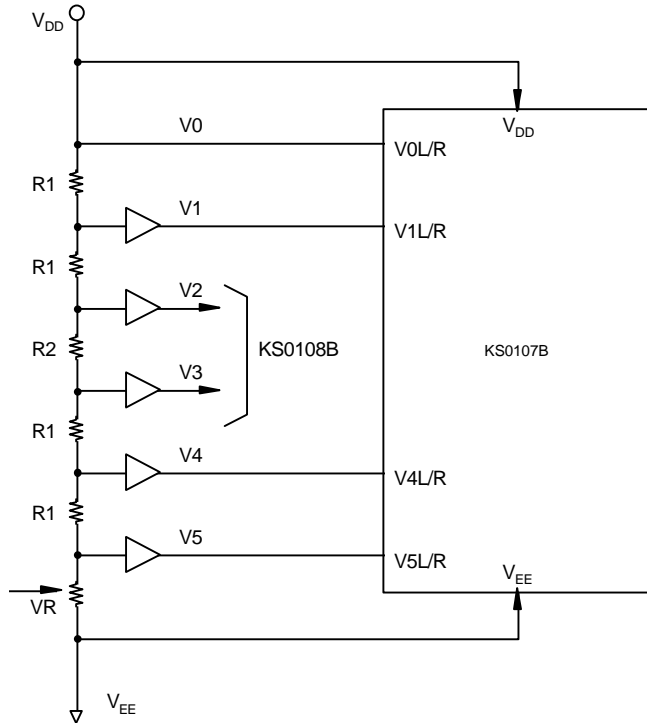
- relation of CL2 and DIO1 (DIO2)



(3) 1/48 duty timing (Slave mode)  
 - Condition: PCLK2=L, SHL=H(L)



(4) Power driver circuit



relation of duty & bias

DUTY	BIAS	R div
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

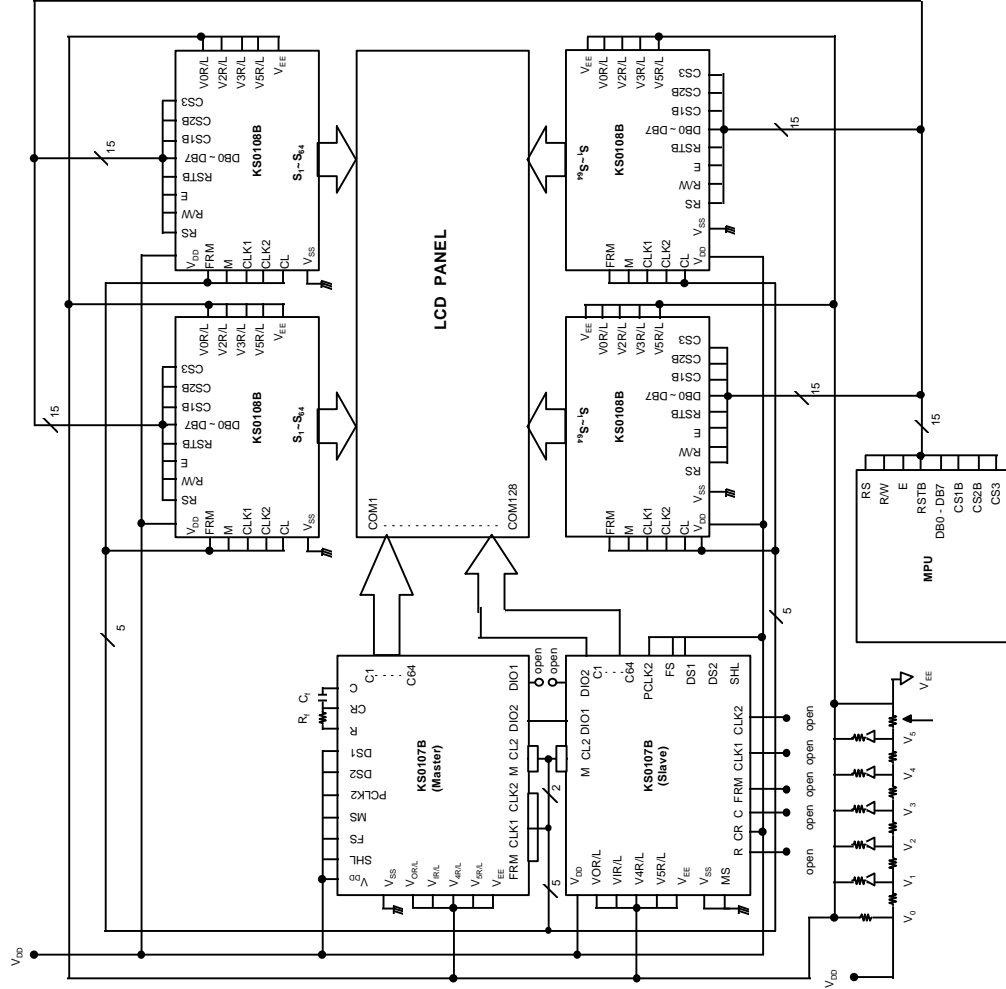
\*When duty factor is 1/48, the value of R1 & R2 should satisfy.

$$R1/(4R1+R2)=1/8$$

$$R1=3K\Omega, R2=12K\Omega$$

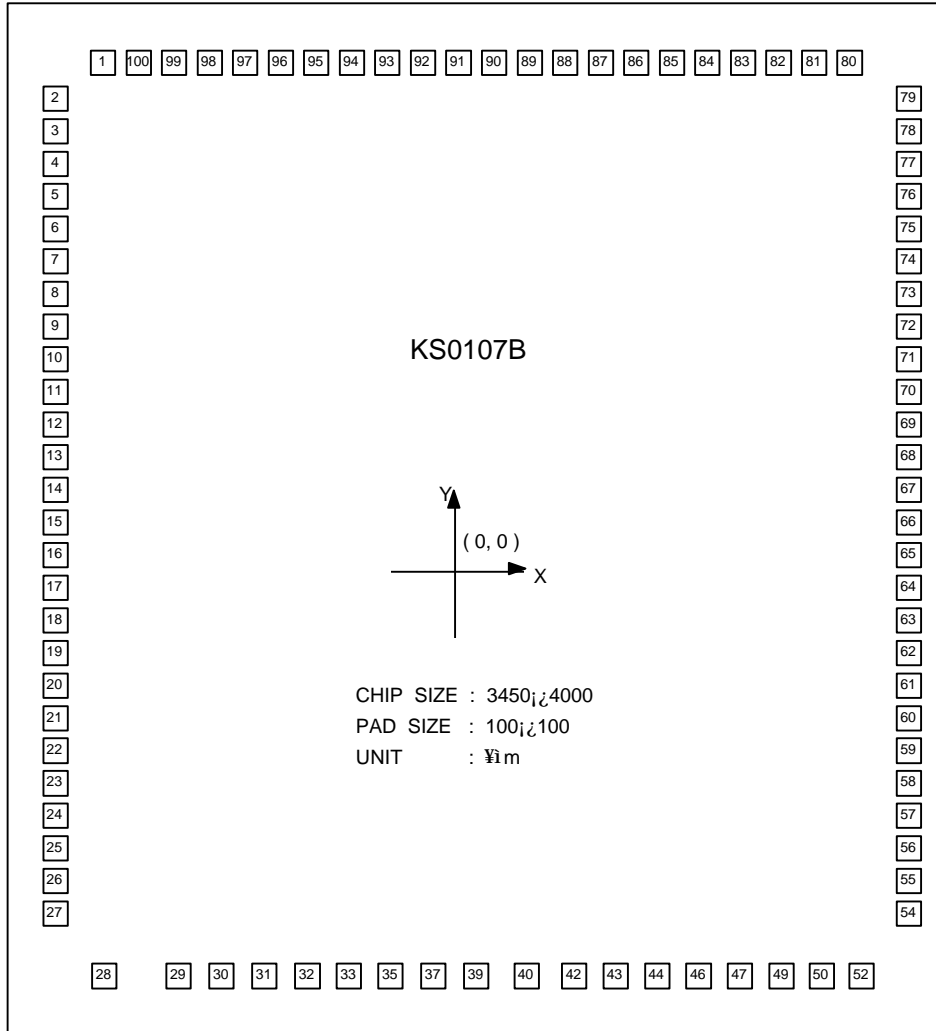
APPLICATION CIRCUIT

-1/128 duty Segment drive(KS0108B) Interface circuit





PAD DIAGRAM



\* There is mark of KS0107B on the center in chip

## PAD LOCATION

UNIT (μ m)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	C22	-1314.5	1775.4	37	CR	-227.6	-1775	77	C46	1500.9	1380
2	C21	-1499.9	1630	39	SHL	-77.6	-1775	78	C45	1500.9	1505
3	C20	-1499.9	1505	40	VSS	113.8	-1775	79	C44	1500.9	1630
4	C19	-1499.9	1380	42	MS	308.7	-1775	80	C43	1310.5	1775.4
5	C18	-1499.9	1255	43	CLK2	458.7	-1775	81	C42	1185.5	1775.4
6	C17	-1499.9	1130	44	CLK1	608.7	-1775	82	C41	1060.5	1775.4
7	C16	-1499.9	1005	46	FRM	758.7	-1775	83	C40	935.5	1775.4
8	C15	-1499.9	880	47	M	908.7	-1775	84	C39	810.5	1775.4
9	C14	-1499.9	775	49	PCLK2	1058.7	-1775	85	C38	685.5	1775.4
10	C13	-1499.9	630	50	DIO2	1208.7	-1775	86	C37	560.5	1775.4
11	C12	-1499.9	505	52	CL2	1358.7	-1775	87	C36	435.5	1775.4
12	C11	-1499.9	380	54	VOR	1500.9	-1495	88	C35	310.5	1775.4
13	C10	-1499.9	255	55	V5R	1500.9	-1370	89	C34	185.5	1775.4
14	C9	-1499.9	130	56	V4R	1500.9	-1245	90	C33	60.5	1775.4
15	C8	-1499.9	5	57	V1R	1500.9	-1120	91	C32	-64.5	1775.4
16	C7	-1499.9	-120	58	VEE	1500.9	-995	92	C31	-189.5	1775.4
17	C6	-1499.9	-245	59	C64	1500.9	-870	93	C30	-314.5	1775.4
18	C5	-1499.9	-370	60	C63	1500.9	-745	94	C29	-439.5	1775.4
19	C4	-1499.9	-495	61	C62	1500.9	-620	95	C28	-564.5	1775.4
20	C3	-1499.9	-620	62	C61	1500.9	-495	96	C27	-689.5	1775.4
21	C2	-1499.9	-745	63	C60	1500.9	-370	97	C26	-814.5	1775.4
22	C1	-1499.9	-870	64	C59	1500.9	-245	98	C25	-939.5	1775.4
23	VEE	-1499.9	-995	65	C58	1500.9	-120	99	C24	-1064.5	1775.4
24	V1L	-1499.9	-1120	66	C57	1500.9	5	100	C23	-1189.5	1775.4
25	V4L	-1499.9	-1245	67	C56	1500.9	130				
26	V5L	-1499.9	-1370	68	C55	1500.9	255				
27	VOL	-1499.9	-1495	69	C54	1500.9	380				
28	VDD	-1345.6	-1775	70	C53	1500.9	505				
29	DIO1	-1127.6	-1775	71	C52	1500.9	630				
30	FS	-979.6	-1775	72	C51	1500.9	755				
31	DS1	-827.6	-1775	73	C50	1500.9	880				
32	DS2	-677.6	-1775	74	C49	1500.9	1005				
33	C	-527.6	-1775	75	C48	1500.9	1130				
35	R	-377.6	-1775	76	C47	1500.9	1255				