Version : 0.1

TFT-LCD CONTROLLER LSI(PVI-2003A)

SPECIFICATION

MODEL NAME. : PVI-2003A

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By

Prepared By

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Date : Mar/24/2005

Content:

Appendix

1. General description

The PVI-2003A is timing controller IC to control PVI OA type TFT LCD modules. This IC generates all kind of control timing signals to the LCD source drivers and gate drivers. Also this IC provides different display mode.

2. Feature

*Support OA video system.
*Support multiple resolution mode
(320* 96,480*480,HVGA,VGA-350,VGA-400,VGA,WVGA,SVGA).
*Support single port RGB driver IC.
*Support DENB/SYNC mode auto-detect.
*Provide timing scan for left/right and up/down shift control.
*Dot inversion driving method.
*Package:TQFP-64 pin(0.5mm pitch).
*Single power supplies:+3.3V
*0.35u CMOS process,3.3V for core ,3.3/5V for input PAD and 3.3V for output PAD.

3. Pin assignment

Pin no.	Pin name	I/O	Remark	Pin No.	Pin name	I/O	Remark
1	RESET	I	Schmitt	33	RO[5]	O	6mA
2	SEL_I_DATA	I	Pull down	34	RO[4]	O	6mA
3	STV2	O	3-state(2mA)	35	RO[3]	O	6mA
4	OEV	O	2mA	36	RO[2]	O	6mA
5	CKV	O	2mA	37	RO[1]	O	6mA
6	UD	I	Pull up	38	RO[0]	O	6mA
7	RL	I	Pull up	39	VSS	I	Ground
8	STV1	O	3-state(2mA)	40	HSYNC	I	
9	SPOL	O	2mA	41	VSYNC	I	
10	POL	O	2mA	42	DENB	I	
11	STB	O	2mA	43	BI[5]	I	
12	STH1	O	3-state(2mA)	44	BI[4]	I	
13	STH2	O	3-state(2mA)	45	BI[3]	I	
14	SEL[2]	I	Pull up	46	BI[2]	I	
15	SEL[1]	I	Pull down	47	BI[1]	I	
16	SEL[0]	I	Pull down	48	BI[0]	I	
17	VDD	I	3.3V	49	VSS	I	Ground
18	OCLK	O	6mA	50	GI[5]	I	
19	BO[5]	O	6mA	51	GI[4]	I	
20	BO[4]	O	6mA	52	GI[3]	I	
21	BO[3]	O	6mA	53	GI[2]	I	
22	BO[2]	O	6mA	54	GI[1]	I	
23	BO[1]	O	6mA	55	GI[0]	I	
24	BO[0]	O	6mA	56	RI[5]	I	
25	VSS	I	Ground	57	RI[4]	I	
26	GO[5]	O	6mA	58	RI[3]	I	
27	GO[4]	O	6mA	59	RI[2]	I	
28	GO[3]	O	6mA	60	RI[1]	I	
29	GO[2]	O	6mA	61	RI[0]	I	
30	GO[1]	O	6mA	62	TEST	I	
31	GO[0]	O	6mA	63	ICLK	I	
32	VDD	I	3.3V	64	VDD	I	3.3V

4. Pin description

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>RESET</td><td>I</td><td>Reset pin in ASIC
1.RESET=H : normal state.
2.RESET=L : reset state.</td><td></td></tr>
<tr><td>2</td><td>SEL_I_DATA</td><td>I</td><td>Select RI,GI,BI data conversion
1.SEL_I_DATA=L : normal RI,GI,BI data
2.SEL_I_DATA=H : reverse RI,GI,BI data</td><td>Note 5</td></tr>
<tr><td>3</td><td>STV2</td><td>O</td><td>Gate driver start pulse
1. UD=L: STV2 is output pin of start pulse.
2. UD=H: STV2 is in high impedance state.</td><td>Note 2</td></tr>
<tr><td>4</td><td>OEV</td><td>O</td><td>Output enable control signal for gate driver
OEV=H : gate driver output equal VEE.</td><td></td></tr>
<tr><td>5</td><td>CKV</td><td>O</td><td>Gate driver shift clock</td><td></td></tr>
<tr><td>6</td><td>UD</td><td>I</td><td>Select up/down direction
1.UD=H : normal scan.
2.UD=L : reverse scan.</td><td>Note 2</td></tr>
<tr><td>7</td><td>RL</td><td>I</td><td>Select left/right direction
1.RL=H : normal scan.
2.RL=L : reverse scan.</td><td>Note 3</td></tr>
<tr><td>8</td><td>STV1</td><td>O</td><td>Gate driver start pulse
1.UD=H: STV1 is output pin of start pulse.
2.UD=L: STV1 is in high impedance state.</td><td>Note 2</td></tr>
<tr><td>9</td><td>SPOL</td><td>O</td><td>Source driver 2-line polarity inverting.</td><td>Note 4</td></tr>
<tr><td>10</td><td>POL</td><td>O</td><td>Source driver line polarity inverting.</td><td>Note 4</td></tr>
<tr><td>11</td><td>STB</td><td>O</td><td>Source driver latch pulse(high active).</td><td></td></tr>
<tr><td>12</td><td>STH1</td><td>O</td><td>Source driver start pulse
1.RL=H : STH1 is output pin of start pulse.
2.RL=L : STH1 is in high impedance state.</td><td>Note 3</td></tr>
<tr><td>13</td><td>STH2</td><td>O</td><td>Source driver start pulse
1.RL=L : STH2 is output pin of start pulse.
2.RL=H : STH2 is in high impedance state.</td><td>Note 3</td></tr>
<tr><td>14
15
16</td><td>SEL[2]
SEL[1]
SEL[0]</td><td>I
I
I</td><td>Select display mode
<table>
<tr><th>SEL[2]</th><th>SEL[1]</th><th>SEL[0]</th><th>Display</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>320*96</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>VGA-350,VGA-400,VGA
(for 642 channel source driver)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>480*480</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>SVGA</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>VGA-350,VGA-400,VGA</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>WVGA</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>HVGA</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>HVGA
(for 642 channel source driver)</td></tr>
</table></td><td>Note 4</td></tr>
<tr><td>17</td><td>VDD</td><td>I</td><td>Power 3.3V</td><td></td></tr>
<tr><td>18</td><td>OCLK</td><td>O</td><td>Source driver shift clock</td><td></td></tr>
<tr><td>19
20</td><td>BO[5]
BO[4]</td><td>O
O</td><td>Blue color</td><td></td></tr>
</table>

21 22 23 24	BO[3] BO[2] BO[1] BO[0]	O O O O		
25	VSS	I	Ground	
26 27 28 29 30 31	GO[5] GO[4] GO[3] GO[2] GO[1] GO[0]	O O O O O O	Green color	
32	VDD	I	Power 3.3V	
33 34 35 36 37 38	RO[5] RO[4] RO[3] RO[2] RO[1] RO[0]	O O O O O O	Red color	
39	VSS	I	Ground	
40	HSYNC	I	Horizontal sync signal in SYNC mode	Note 1
41	VSYNC	I	Vertical sync signal in SYNC mode	Note 1
42	DENB	I	Data enable signal in DENB mode	Note 1
43 44 45 46 47 48	BI[5] BI[4] BI[3] BI[2] BI[1] BI[0]	I I I I I I	Blue color	
49	VSS	I	Ground	
50 51 52 53 54 55	GI[5] GI[4] GI[3] GI[2] GI[1] GI[0]	I I I I I I	Green color	
56 57 58 59 60 61	RI[5] RI[4] RI[3] RI[2] RI[1] RI[0]	I I I I I I	Red color	
62	TEST	I	Select AC/DC test TEST=H : AC/DC test mode. TEST=L : normal mode.	
63	ICLK	I	System clock	
64	VDD	I	Power 3.3V	

Note 1: If PVI-2003A is set in SYNC(HSYNC+VSYNC)mode, DENB pin have to be always hold low voltage.

When PVI-2003A's DENB pin receive AC toggle signal, then ASIC is set in DENB mode.

Note 2: UD control gate driver up/down direction

1.UD=H : STV1 →G1→G2→G3→G4→G5→G6→G7→G8→------→STV2

2.UD=L : STV1 ←G1←G2←G3←G4←G5←G6←G7←G8←----- ←STV2

Note 3: RL control source driver right/left direction

1.RL=H : STH1→S1→S2→S3→S4→S5→S6→S7→S8→------→STH2

2.RL=L : STH1←S1←S2←S3←S4←S5←S6←S7←S8←------←STH2

Note 4:

SVGA	800*600 panel resolution
WVGA	800*480 panel resolution
VGA	640*480 panel resolution
VGA-350(SYNC mode)	640*480 panel resolution
VGA-400(SYNC mode)	640*480 panel resolution
HVGA	640*240 panel resolution
480*480	480*480 panel resolution
320*96	320*96 panel resolution

When ASIC use VGA-350 or VGA-400 mode, then SPOL become POL.

SYNC mode	HSYNC polarity	VSYNC polarity
VGA-350	Positive	Negative
VGA-400	Negative	Positive
VGA	Positive Negative	Positive Negative
SVGA WVGA HVGA 480*480 320*96	Negative Negative Negative Negative Negative	Negative Negative Negative Negative Negative

Note 5: select RI,GI,BI data conversion

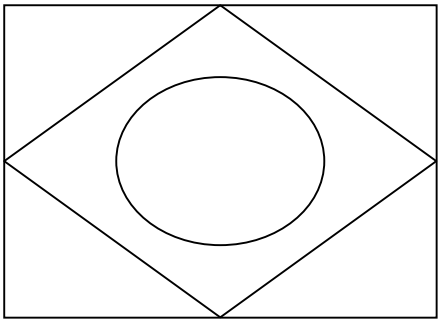
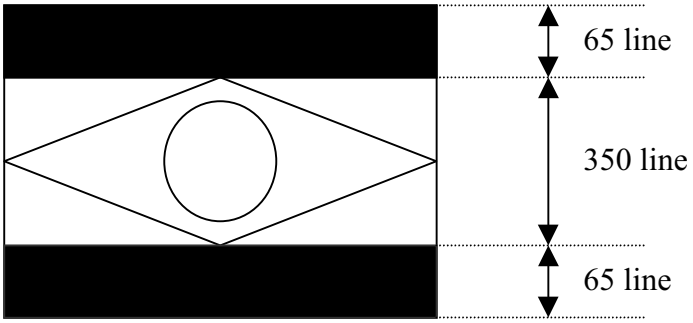
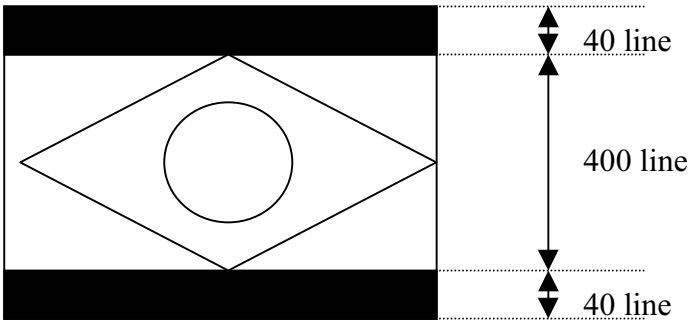
1.SEL_I_DATA=H:

RI[5..0] become BI[0..5]

GI[5..0] become GI[0..5]

BI[5..0] become RI[0..5]

5. Display mode

Display mode	Display characteristic
SVGA(full screen) WVGA(full screen) VGA(full screen) HVGA(full screen) 480*480(full screen) 320*96(full screen)	
VGA-350	
VGA-400	

6. Electrical characteristic

6.1 Absolute maximum rating

Parameter	Symbol	limit	Unit	Remark
Power supply voltage	VDD	VSS-0.3 to 4.0	V	
Input voltage	Vin	VSS-0.3 to 7.0	V	
Output voltage	Vout	VSS-0.3 to VDD+0.5	V	
Storage temperature	Tstg	-65 to 150	℃	

6.2 Recommended operating condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage	VDD	3.0	3.3	3.6	V	
Input voltage	Vin	0	-	5.5	V	
Operating temperature	Toper	-40	-	85	℃	

6.3 General DC characteristic

Parameter	Symbol	condition	Min.	Typ.	Max.	Unit	Remark
Input leakage current	I_{LC}	VDD=max V_{IH}=VDD V_{IL}=0V	-1	-	1	uA	
Logic input low voltage	V_{IL}	VDD=min	-	-	0.8	V	
Logic input high voltage	V_{IH}	VDD=max	2.0	-	-	V	
Schmitt input low voltage	V_{SIL}	VDD=min	0.6	-	1.8	V	
Schmitt input high voltage	V_{SIH}	VDD=max	1.1	-	2.4	V	
Output low voltage	V_{OL}	VDD=min	VSS-0.4	-	-	V	
Output high voltage	V_{OH}	VDD=max	-	-	VDD+0.4	V	
Input pull up/down resistance	R_I	V_{IL}=0V or V_{IH}=VDD	-	50	-	kΩ	

7. Timing condition(reference A. The timing diagram in page 35)

7.1 SVGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	40	-	MHz	
		tc	-	25	-	ns	
HSYNC	Period	Hp	-	26.4	-	us	
			-	1056	-	tc	
	Display period	Hdp	-	800	-	tc	
	Pulse width	Hpw	-	128	-	tc	
	Back-porch	Hbp	-	86	-	tc	
	Front-porch	Hfp	-	42	-	tc	
	Hpw+Hbp		-	214	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.579	-	ms	
			-	628	-	Hp	
	Display period	Vdp	-	600	-	Hp	
	Pulse width	Vpw	-	4	-	Hp	
	Back-porch	Vbp	-	23	-	Hp	
	Front-porch	Vfp	-	1	-	Hp	
	Vpw+Vbp		-	27	-	Hp	
DENB	Horizontal scanning period	T1	-	1056	-	tc	
	Horizontal display period	T2	-	800	-	tc	
	Vertical display period	T3	-	600	-	T1	
	Frame cycling period	T4	-	628	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	25	-	ns	
Tod	25	-	-	ns	
Tsth	-	25	-	ns	
Tstb	-	2	-	us	
Tpol	-	26.4	-	us	
Tspol	-	52.8	-	us	
Tstv	-	28.5	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

7.2 WVGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	32	-	MHz	
		tc	-	31.25	-	ns	
HSYNC	Period	Hp	-	33	-	us	
			-	1056	-	tc	
	Display period	Hdp	-	800	-	tc	
	Pulse width	Hpw	-	128	-	tc	
	Back-porch	Hbp	-	86	-	tc	
	Front-porch	Hfp	-	42	-	tc	
	Hpw+Hbp		-	214	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	17.325	-	ms	
			-	525	-	Hp	
	Display period	Vdp	-	480	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	33	-	Hp	
	Front-porch	Vfp	-	10	-	Hp	
	Vpw+Vbp		-	35	-	Hp	
DENB	Horizontal scanning period	T1	-	1056	-	tc	
	Horizontal display period	T2	-	800	-	tc	
	Vertical display period	T3	-	480	-	T1	
	Frame cycling period	T4	-	525	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	31.25	-	ns	
Tod	31.25	-	-	ns	
Tsth	-	31.25	-	ns	
Tstb	-	2.5	-	us	
Tpol	-	33	-	us	
Tspol	-	66	-	us	
Tstv	-	35.625	-	us	
Tckv	-	7.5	-	us	
Toev	-	6.25	-	us	

7.3 VGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	-	96	-	tc	
	Back-porch	Hbp	-	48	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	144	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			-	525	-	Hp	
	Display period	Vdp	-	480	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	33	-	Hp	
	Front-porch	Vfp	-	10	-	Hp	
	Vpw+Vbp		-	35	-	Hp	
DENB	Horizontal scanning period	T1	-	800	-	tc	
	Horizontal display period	T2	-	640	-	tc	
	Vertical display period	T3	-	480	-	T1	
	Frame cycling period	T4	-	525	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40	-	ns	
Tod	40	-	-	ns	
Tsth	-	40	-	ns	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

7.4 VGA-350 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	-	96	-	tc	
	Back-porch	Hbp	-	48	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	144	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	14.3	-	ms	
			-	449	-	Hp	
	Display period	Vdp	-	350	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	60	-	Hp	
	Front-porch	Vfp	-	37	-	Hp	
	Vpw+Vbp		-	62	-	Hp	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40	-	ns	
Tod	40	-	-	ns	
Tsth	-	40	-	ns	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

7.5 VGA-400 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	-	96	-	tc	
	Back-porch	Hbp	-	48	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	144	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	14.3	-	ms	
			-	449	-	Hp	
	Display period	Vdp	-	400	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	35	-	Hp	
	Front-porch	Vfp	-	12	-	Hp	
	Vpw+Vbp		-	37	-	Hp	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40	-	ns	
Tod	40	-	-	ns	
Tsth	-	40	-	ns	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

7.6 HVGA

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	12.5	-	MHz	
		tc	-	80	-	ns	
HSYNC	Period	Hp	-	64	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	-	96	-	tc	
	Back-porch	Hbp	-	48	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	144	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			-	262	-	Hp	
	Display period	Vdp	-	240	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	15	-	Hp	
	Front-porch	Vfp	-	5	-	Hp	
	Vpw+Vbp		-	17	-	Hp	
DENB	Horizontal scanning period	T1	-	800	-	tc	
	Horizontal display period	T2	-	640	-	tc	
	Vertical display period	T3	-	240	-	T1	
	Frame cycling period	T4	-	262	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	80	-	ns	
Tod	80	-	-	ns	
Tsth	-	80	-	ns	
Tstb	-	6.4	-	us	
Tpol	-	64	-	us	
Tspol	-	128	-	us	
Tstv	-	78.4	-	us	
Tckv	-	19.2	-	us	
Toev	-	16	-	us	

7.7 480*480 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	20	-	MHz	
		tc	-	50	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	640	-	tc	
	Display period	Hdp	-	480	-	tc	
	Pulse width	Hpw	-	96	-	tc	
	Back-porch	Hbp	-	48	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	144	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			-	525	-	Hp	
	Display period	Vdp	-	480	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	33	-	Hp	
	Front-porch	Vfp	-	10	-	Hp	
	Vpw+Vbp		-	35	-	Hp	
DENB	Horizontal scanning period	T1	-	640	-	tc	
	Horizontal display period	T2	-	480	-	tc	
	Vertical display period	T3	-	480	-	T1	
	Frame cycling period	T4	-	525	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	50	-	ns	
Tod	50	-	-	ns	
Tsth	-	50	-	ns	
Tstb	-	4	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	41	-	us	
Tckv	-	7.5	-	us	
Toev	-	6.25	-	us	

7.8 320*96 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	2.5	-	MHz	
		tc	-	400	-	ns	
HSYNC	Period	Hp	-	160	-	us	
			-	400	-	tc	
	Display period	Hdp	-	320	-	tc	
	Pulse width	Hpw	-	48	-	tc	
	Back-porch	Hbp	-	16	-	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		-	64	-	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.6	-	ms	
			-	104	-	Hp	
	Display period	Vdp	-	96	-	Hp	
	Pulse width	Vpw	-	2	-	Hp	
	Back-porch	Vbp	-	2	-	Hp	
	Front-porch	Vfp	-	4	-	Hp	
	Vpw+Vbp		-	4	-	Hp	
DENB	Horizontal scanning period	T1	-	400	-	tc	
	Horizontal display period	T2	-	320	-	tc	
	Vertical display period	T3	-	96	-	T1	
	Frame cycling period	T4	-	104	-	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

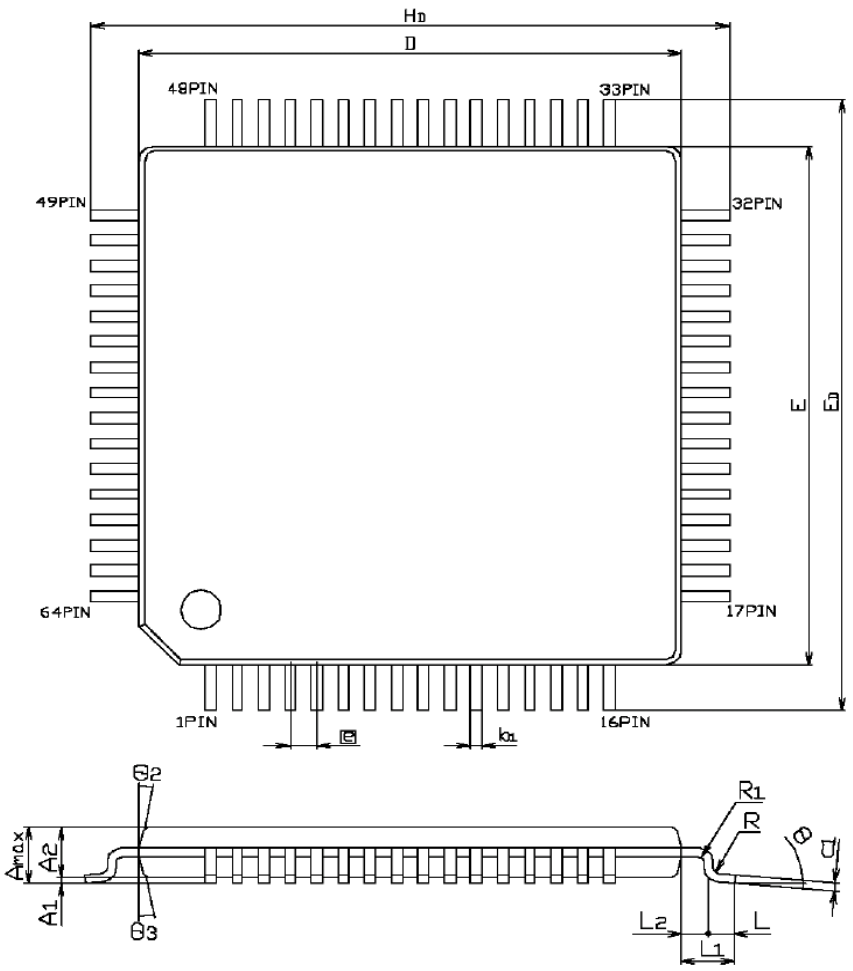
b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	400	-	ns	
Tod	400	-	-	ns	
Tsth	-	400	-	ns	
Tstb	-	32	-	us	
Tpol	-	160	-	us	
Tspol	-	320	-	us	
Tstv	-	208	-	us	
Tckv	-	60	-	us	
Toev	-	50	-	us	

8. Reliability test item

No.	Test item	condition	remark
1	High temperature storage	Ta=150℃ 240h	
2	Low temperature storage	Ta=-60℃ 240h	
3	High temperature operation	Ta=85℃ 240h	
4	Low temperature operation	Ta=-40℃ 240h	
5	High temperature and High humidity	Ta=80℃ , 95%RH 240h	operation
6	Heat shock	-30℃, 25℃, 80℃ 200cycle 30min,5min,30min	Non-operation
7	Electrostatic discharge	± 200V,200pF(0Ω) once for each terminal	Non-operation

9. Package information



Symbol	Dimension in Millimeters		
	Min	Nom	Max
* E	10.1	10.2	10.3
* D	10.1	10.2	10.3
Amax			1.2
A1		0.1	
A2	0.9	1	1.1
e		0.5	
* k1	0.17	0.2	0.27
* c1	0.125	0.15	0.2
θ	0°		10°
L	0.3	0.5	0.7
L1		1	
L2		0.5	
HE	11.6	12	12.4
HD	11.6	12	12.4
θ2		15°	
θ3		15°	
R		0.1	
R1		0.1	

*E,D Excluding the tie bar cutting stub.

k1 Lead width of basemetal.

c1 Lead thickness of basemetal.

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	
1.1	1999.12.03	S.HIRAIDE	A.HARA	A.HARA	CORRECTION ARTICLE

TITLE: TQFP13-64PIN [P-TQFP-0064-1010-0.5]

EIAJ ED-7311 S.N CJ

CAD FILE

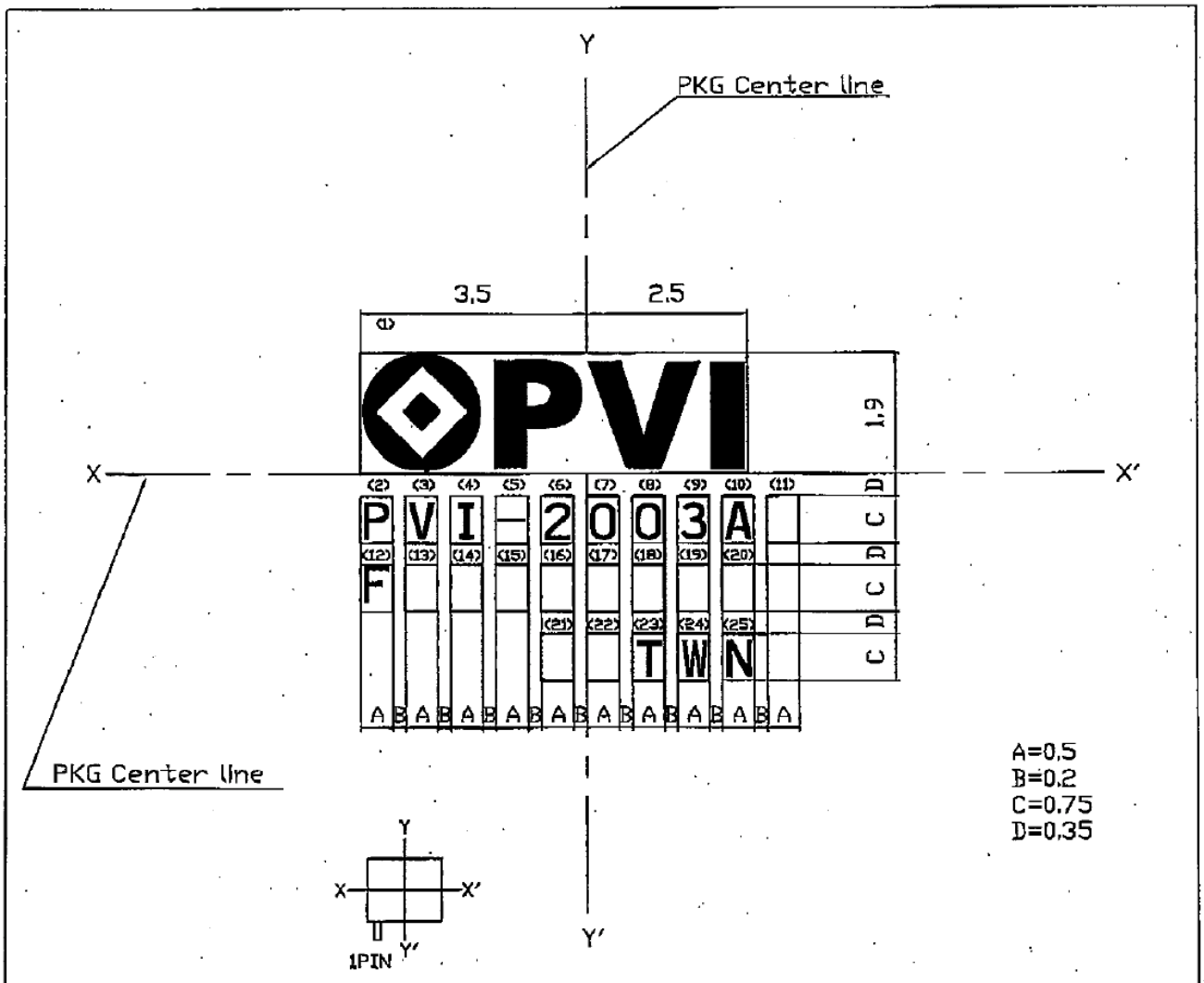
DWG No. 4900-0226

SCALE Free SHEET 1 of 1

SEIKO EPSON CORP.

2900-0002-01(Rev.1.1)

Package Marking



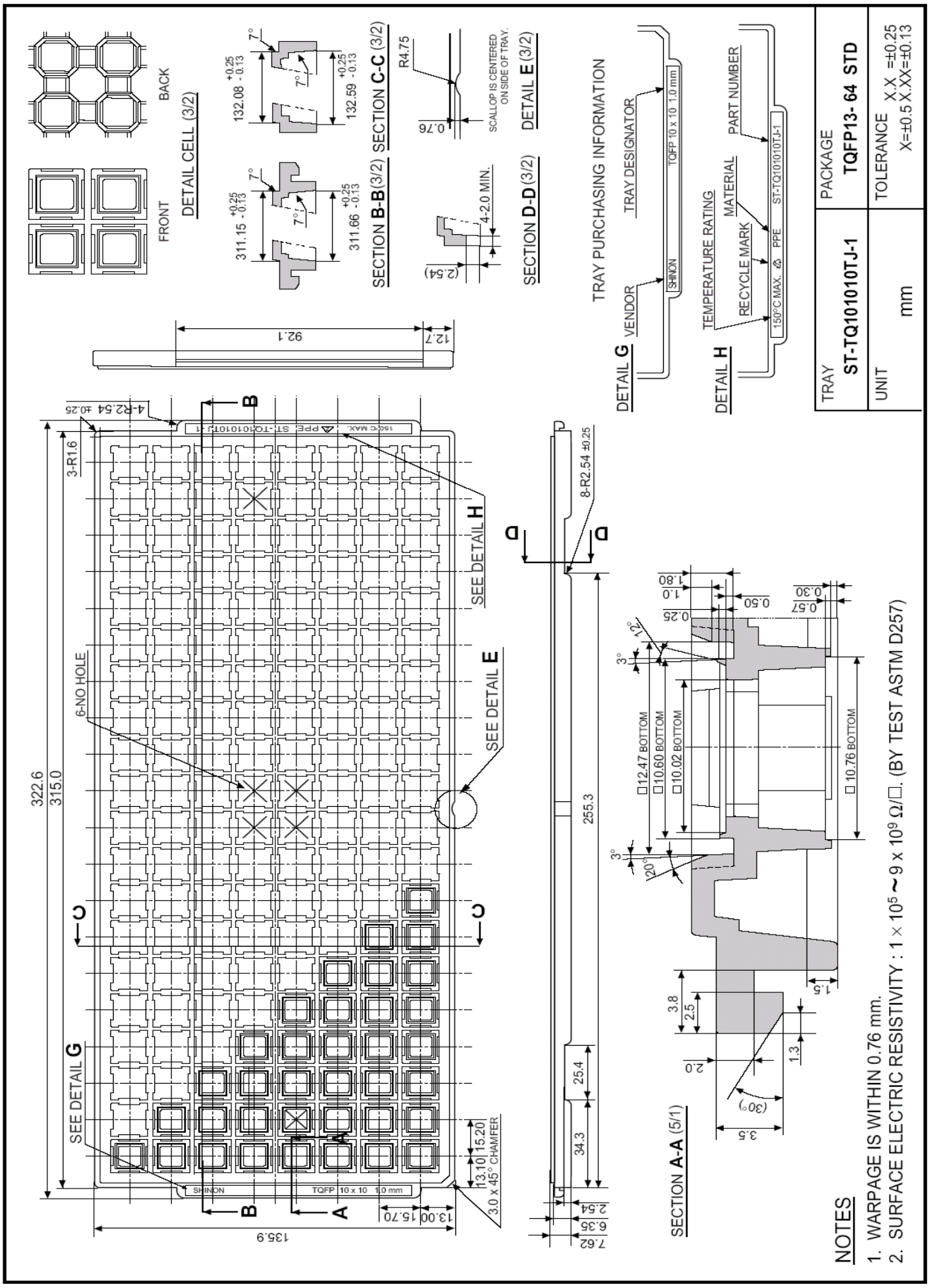
EXPLANATION OF MARK[:FIXED(固定)] S=10/1 1=1mm

ITEM(項目)	No.	NOTE.(備考)
*CUSTOMER MARK(ユーザーマーク)	(1)	REFER TO LOGO TYPE FIXED(指定ロゴ使用)
*「 TWN 」	(21)~(25)	(21),(22) BLANK
*NAME OF GOODS(機種名)	(2)~(11)	(11) BLANK
CONTROL CODE(管理コード)	(12)~(20)	
*「F」	(12)	
YEAR OF MANUFACTURE(製造年)	(13)~(14)	LAST TWO NUMBER OF A.D.(西暦下2桁)
WEEK OF MANUFACTURE(製造週)	(15)~(16)	CALENDAR WEEK OF THE YEAR(1月1日を含む週01より通番)
W/F LOT No.	(17)~(20)	e.g. 0106 → 0106 IC生産管理部門より指定 1254 → 1254 される4桁のウェハロットNo. S352 → S352

TQFP13 用

								NAME	PVI-2003A (S1X56033F00E000)
								PACKAGE TYPE	TQFP13-64PIN
								DEVICE CODE	
1.0			Sato 1/27	Abe 1/27	関 1/27		EST	ASSEMBLY SPEC.	No.
REV.	DATE	DESC.	APPD	CHEKD.	DRAW	CUSTOM	CONTENTS	TEMPLATE.	No. FTQ13H0342

SEIKO EPSON CORP. 0190-0117*付表-5-2*REV.5


BACK
FRONT
DETAIL CELL (3/2)
SECTION B-B (3/2)
SECTION C-C (3/2)
SECTION D-D (3/2)
DETAIL E (3/2)
SCALLOP IS CENTERED ON SIDE OF TRAY.
TRAY PURCHASING INFORMATION
DETAIL G
VENDOR
TRAY DESIGNATOR
SHINON
TQFP 10 x 10 1.0 mm
DETAIL H
TEMPERATURE RATING
MATERIAL
PART NUMBER
RECYCLE MARK
150°C MAX. PPE ST-TQ101010TJ-1
TRAY ST-TQ101010TJ-1
PACKAGE TQFP13- 64 STD
UNIT mm
TOLERANCE X.X =±0.25 X=±0.5 X.XX=±0.13
SEE DETAIL G
SEE DETAIL H
SEE DETAIL E
SECTION A-A (5/1)
6-NO HOLE
3-R1.6
4-R2.54 ±0.25
8-R2.54 ±0.25
322.6
315.0
135.9
255.3
NOTES
1. WARPAGE IS WITHIN 0.76 mm.
2. SURFACE ELECTRIC RESISTIVITY : 1 × 10⁵ ~ 9 x 10⁹ Ω/□. (BY TEST ASTM D257)

10. Usage Precaution

10-1. Storage and handling before opening

Control the storage environment to prevent drastic temperature changes, which can lead to moisture condensation. Do not place any load on the package during storage.

10-2. Hygroscopic indicator monitoring

Because the appearance of normal silica gel do not change when absorbing moisture, a special blue gel manufactured by impregnating silica gel with cobalt chloride($CoCl_2$) is used as moisture absorption indicator. The molecular formula of this gel changes to $CoCl_2 \cdot 6H_2O$(pink) when it has absorbed moisture. Before mounting, you should check the silica gel condition.

10-3. Handling after opening

Do not bring any materials that can generate static electricity (plastic materials, chemical fibers, etc.) into the working area, and periodically check electrostatic conditions. Handle devices only with anti-statically treated materials or in conductive containers. Personnel should use wrist straps or other body grounding means.

10-4. Storage after opening

Due to the properties of the molding resin, plastic packages are prone to moisture absorption, also at room temperature if left for long periods of time. If the package is then inserted in the reflow oven while having absorbed moisture, cracks can develop in the resin, and joint between resin and lead frame can deteriorate. The standard storage periods for SMD packages shown below should therefore not be exceeded.

Table 10.1 Storage conditions after opening moisture proof packing

Storage rank	Storage condition after opening moisture proof packing	Guarantee period after opening moisture proof packing
SE 3	≤30℃/70% RH	Within 168 hours(1 week)

- Storage period before opening a moisture proof packing 12 months at less than ≤30℃/85% RH
- If reflow a package for 2 times, it should be done within storage periods for each package rank
- If the storage period is exceeded or it is undefined, perform baking again before mounting.

  Example : 125℃ for 24 hours (See section 10.5)

10-5. Baking

If the storage period is exceeded after opening, or if the opening data undefined, or if the hygroscopic indicator (blue gel) has turned pink, perform baking as indicated below.

Table 10.2 Baking conditions for surface mount devices

Baking Temperature / Package thickness	125℃
t 〈 2 mm	5 hours
t ≥2 mm	24 hours

Note : Baking may be performed up to maximum of two times

10-6. Soldering conditions

When soldering surface mount devices using an overall soldering method such as reflow or vapor phase soldering, be sure to observe the storage conditions given in Table 10.1, This is important to prevent the possibility of crack and other damage, which increases if plastic package absorb moisture.

10-6-1 Infrared / air reflow

● Temperature profile

The temperature profile of the reflow oven (resin surface temperature) should be controlled as shown in Fig. 10.1

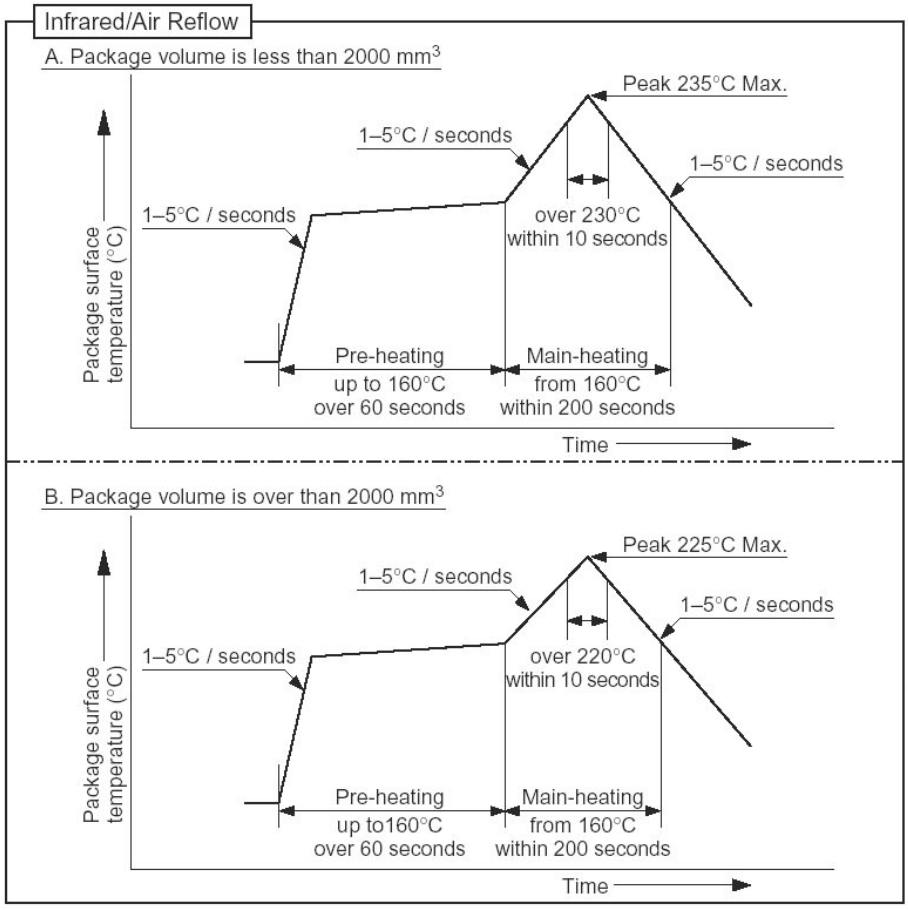


Fig. 10.1 Temperature profile for standard SMD package

● Maximum temperature

The maximum resin surface temperature should be 235 ℃, for a duration of 10 seconds or less. If possible, lower temperatures and shorter times are preferable.

10-6-2 Vapor phase reflow

● Temperature profile

The temperature profile of the vapor phase reflow oven (resin surface temperature) should be controlled as shown in Fig. 10.2

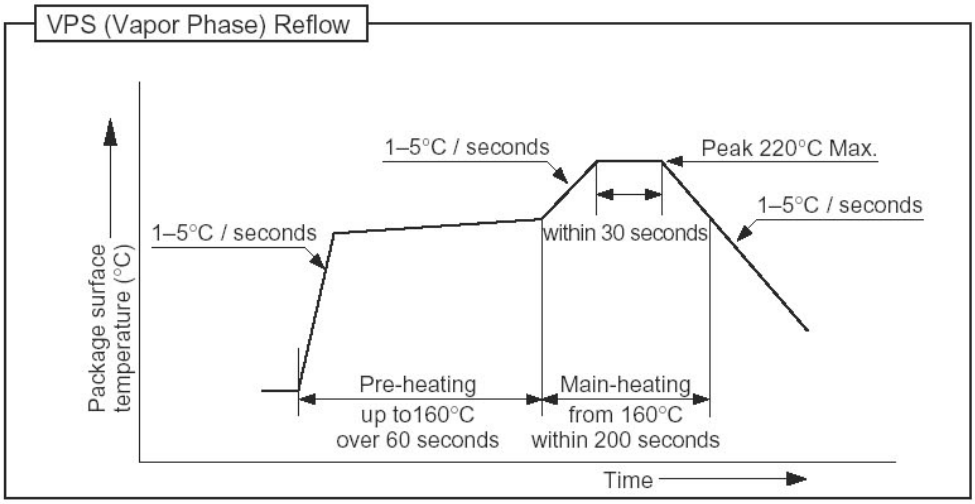


Fig. 10.2 Temperature profile for standard SMD package

● Temperature rise ratio

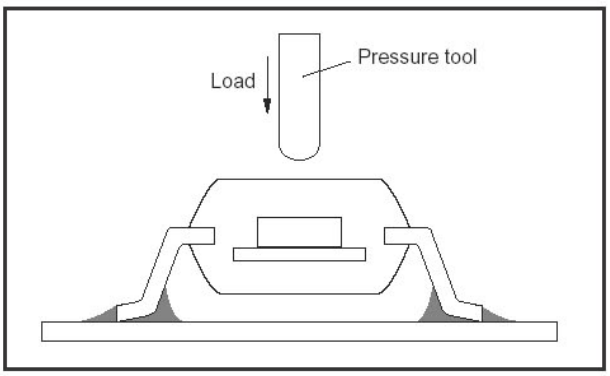
The maximum rise should be kept within 1- 5 ℃/minute, and the curve should be as shallow as possible.

10-6-3 Solder dipping (wave soldering etc)

Because solder dipping cause a drastic change in package temperature which can damage the device, Seiko Epson normally does not approve solder dipping methods for SMD. However, certain SOP with good heat resistance may be mounted using solder dipping.

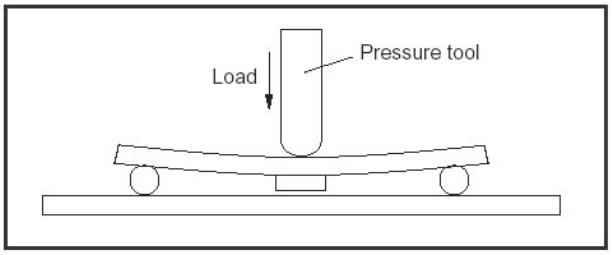
10-7 Mounting Precautions

Mechanical stress during mounting should be minimized (EIAJ-ED-4702)



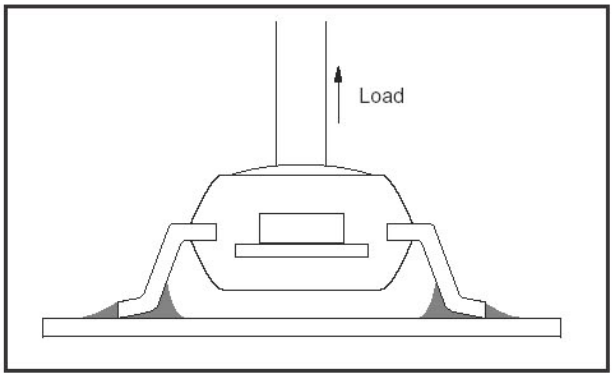
① Package load
The force exerted on the package surface during mounting should not exceed 1 kgf (10 N).

Fig. 10.3 Package Strength



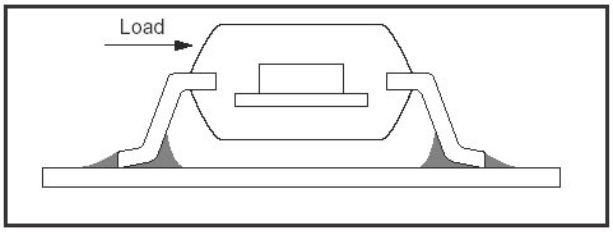
② PCB bending stress
For reasons of solder junction strength, PCB deflection after mounting should not exceed 2 mm.

Fig. 10.4 PCB Bending Strength



③ Pull load
Pull stress (sudden force exerted on the package in vertical up direction) after mounting should not exceed 0.5 kgf (5 N).

Fig. 10.5 Pull Strength



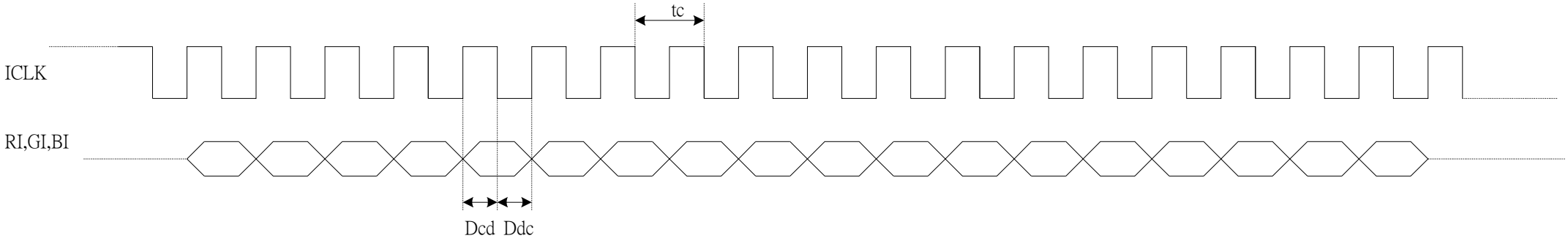
④ Sticking stress
Sticking stress (sudden force exerted on the package in sideways direction) after mounting should not exceed 0.5 kgf (5 N).

Fig. 10.6 Sticking Strength

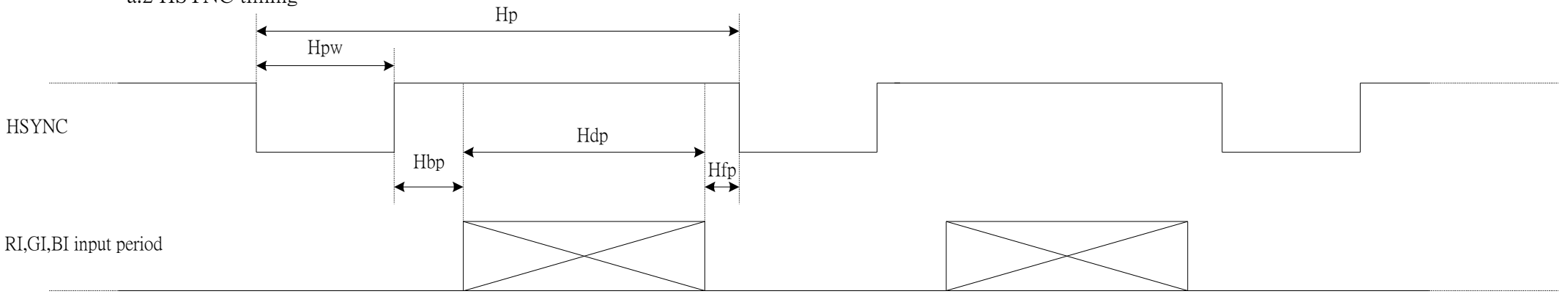
A. The timing diagram

a. Input signal range

a.1 ICLK,RI,GI,BI relationship

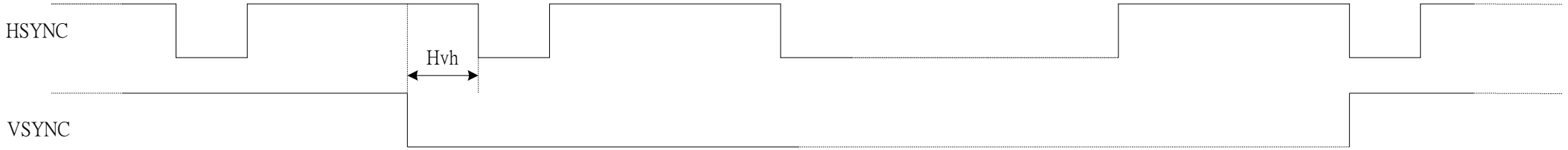


a.2 HSYNC timing

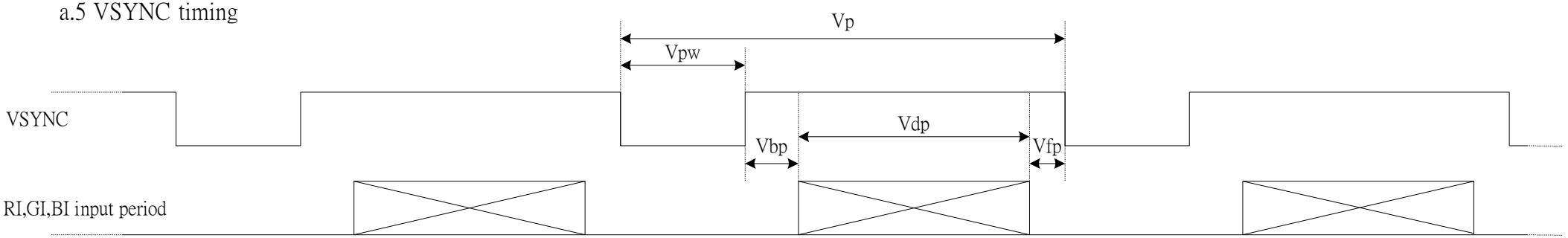


a.3 ICLK,HSYNC relationship

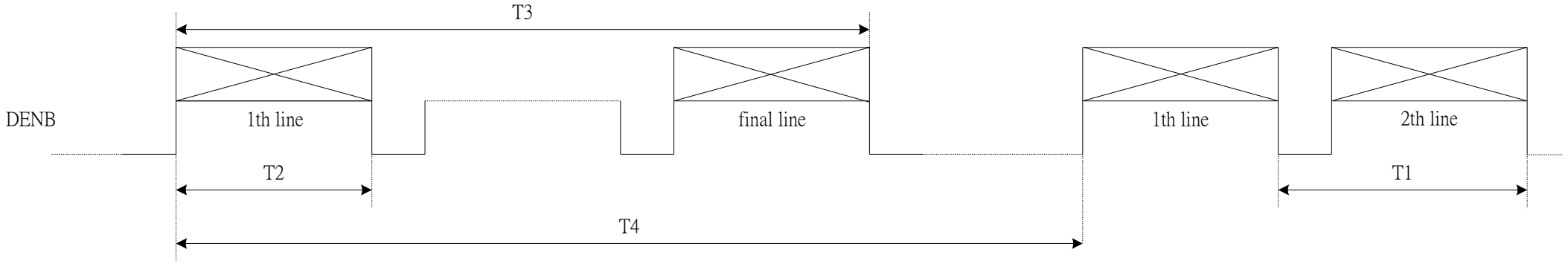
a.4 HSYNC,VSYNC relationship



a.5 VSYNC timing

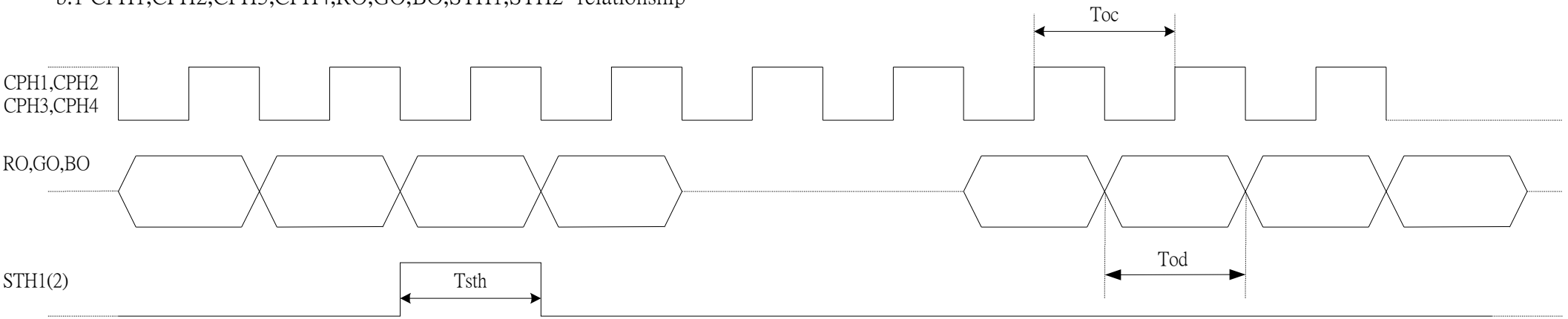


a.6 DENB timing

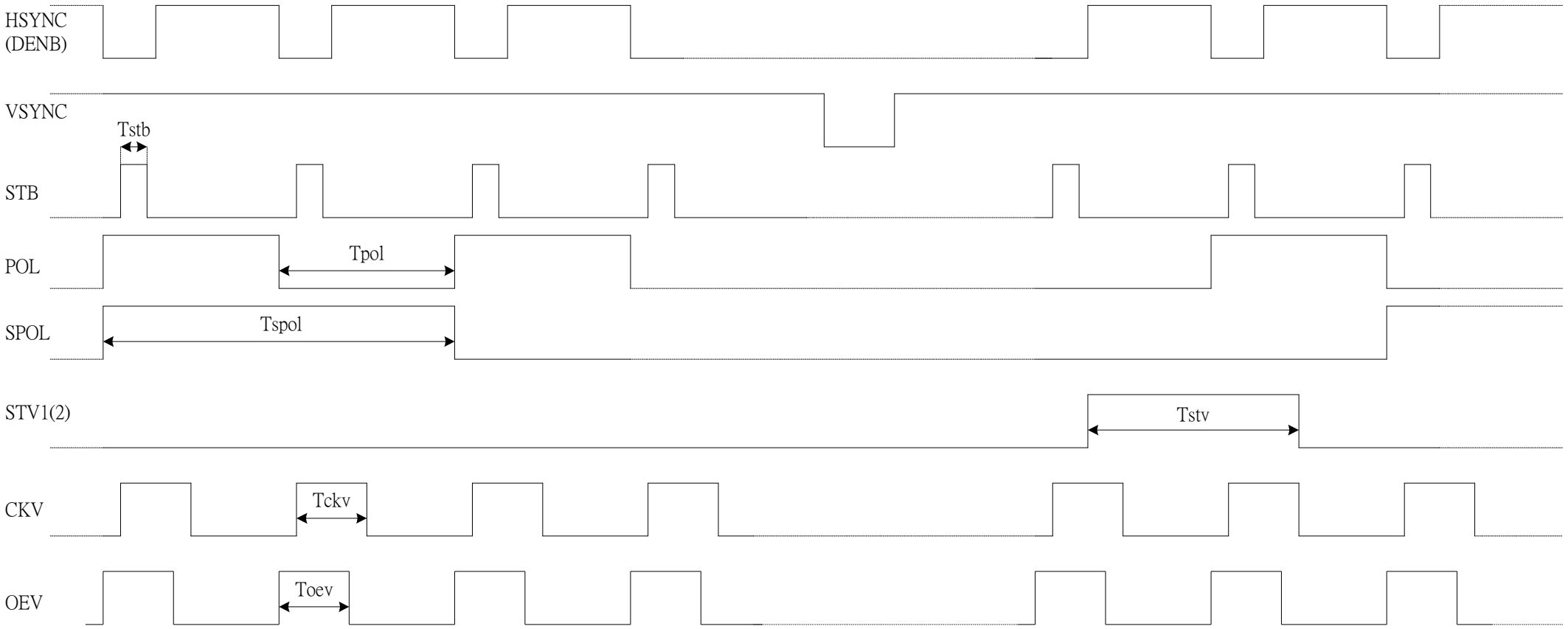


b. Output signal timing(when input signal equal typ. value)

b.1 CPH1,CPH2,CPH3,CPH4,RO,GO,BO,STH1,STH2 relationship

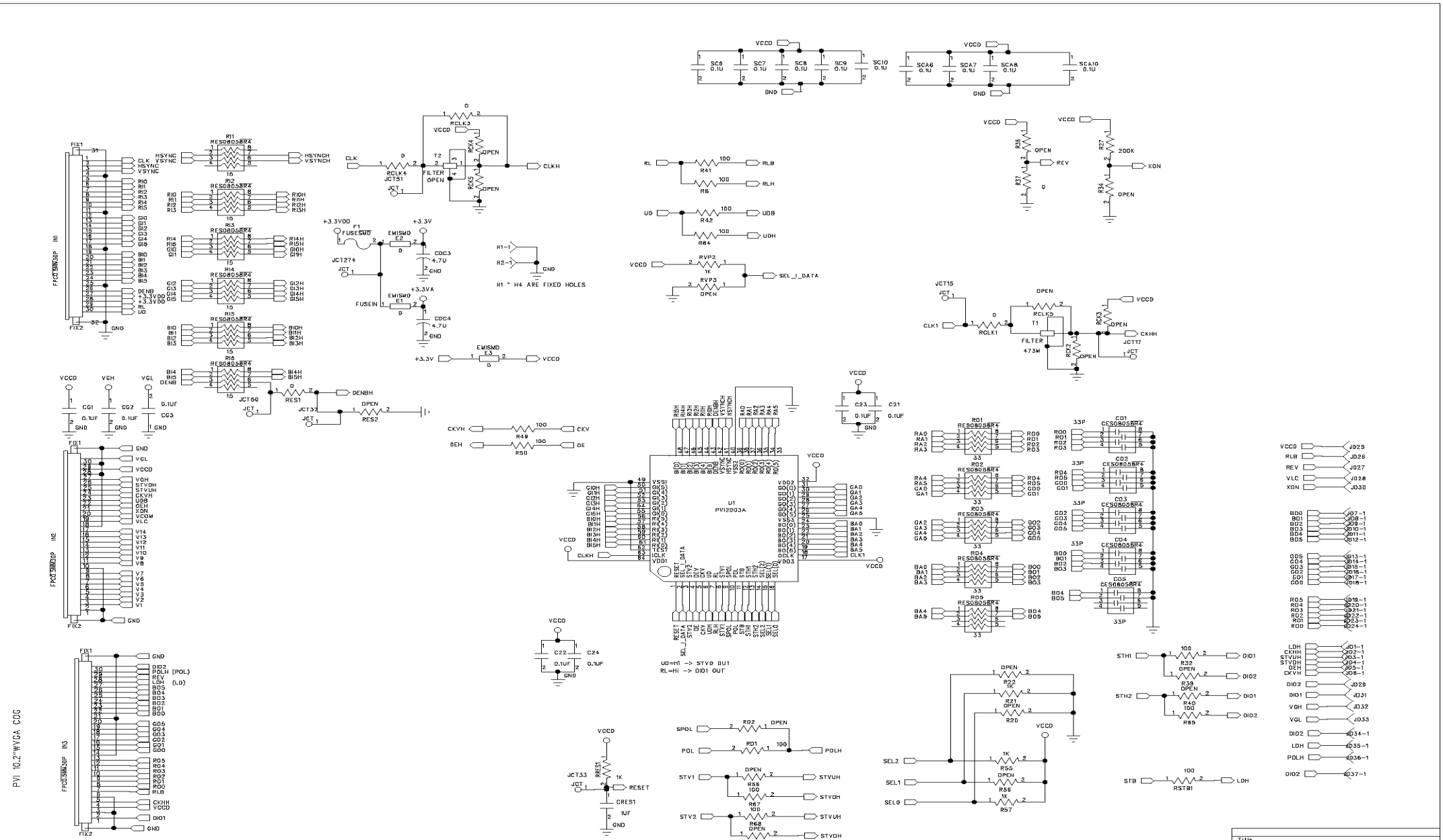


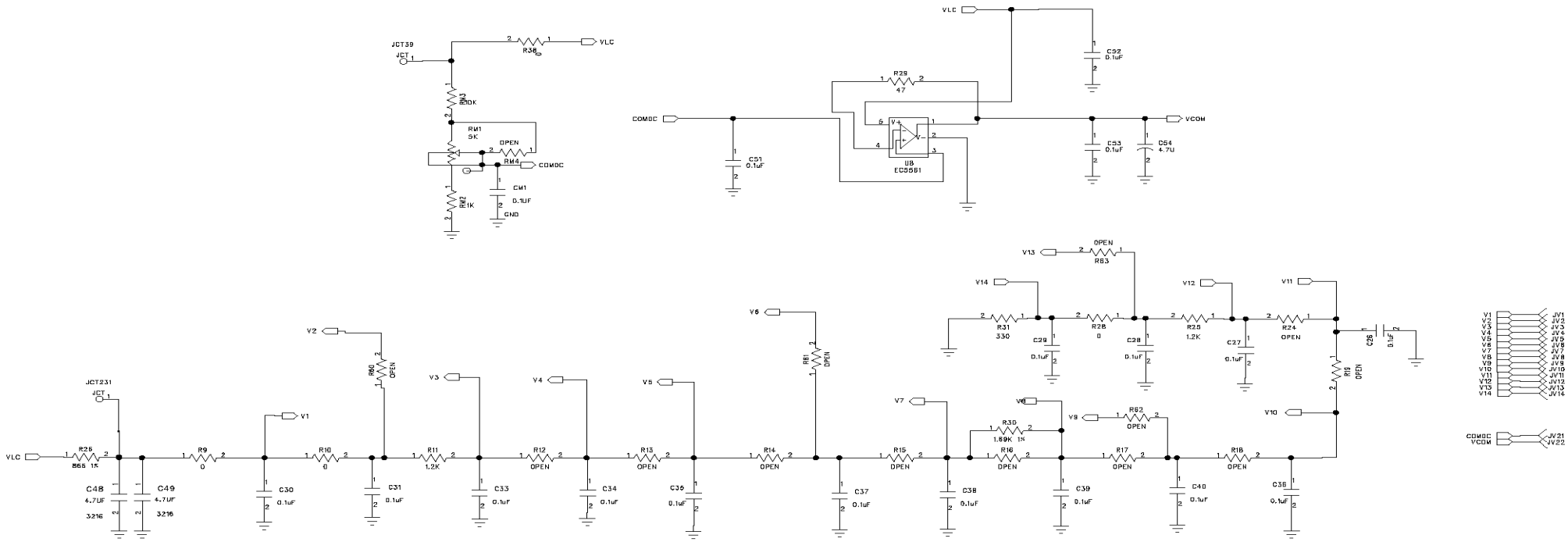
b.2 HSYNC,VSYNC,DENB,STB,POL,SPOL,CKV,OEV,STV1,STV2 relationship



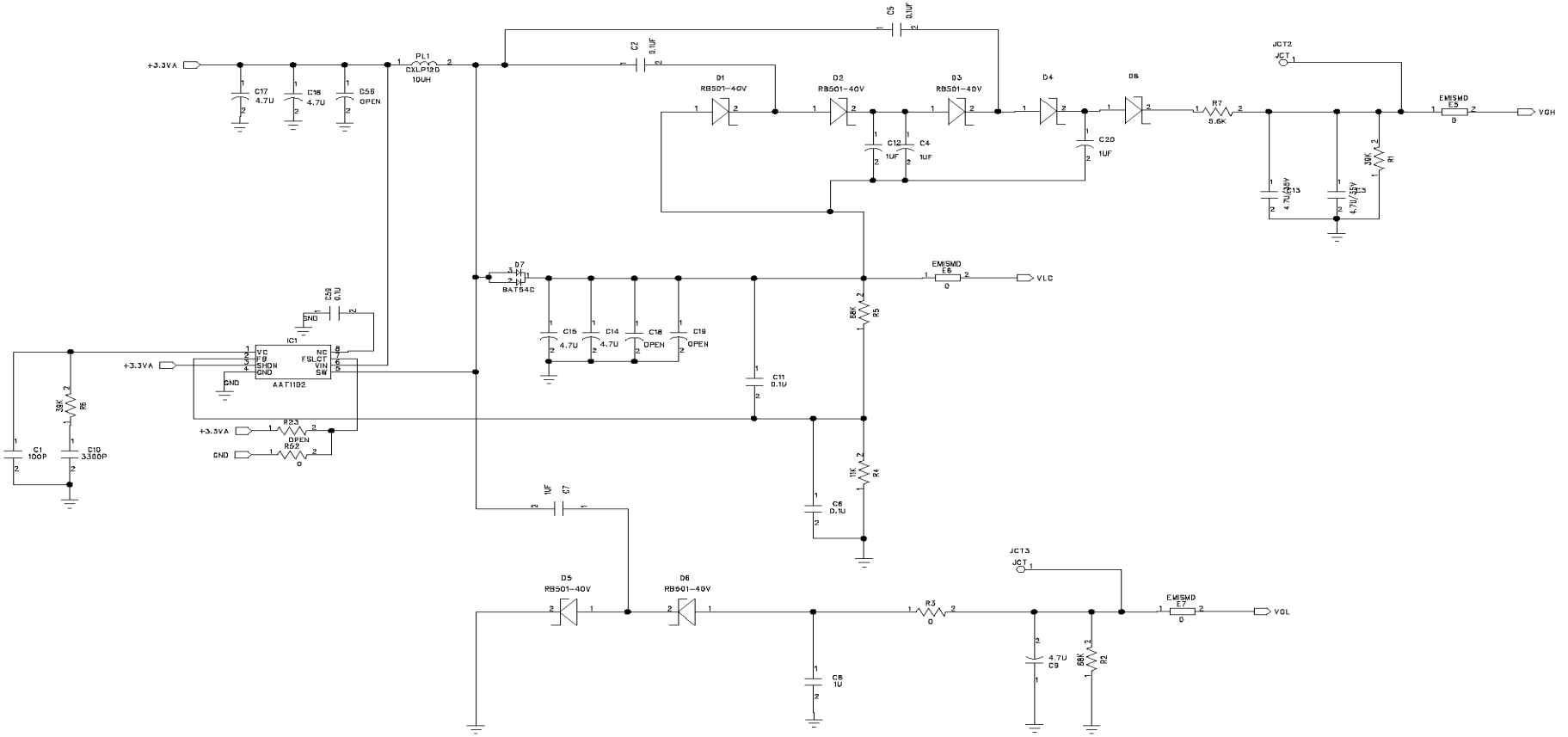
B. Application circuit

a.1 10.2 inch WVGA reference circuit in next three continuous pages.



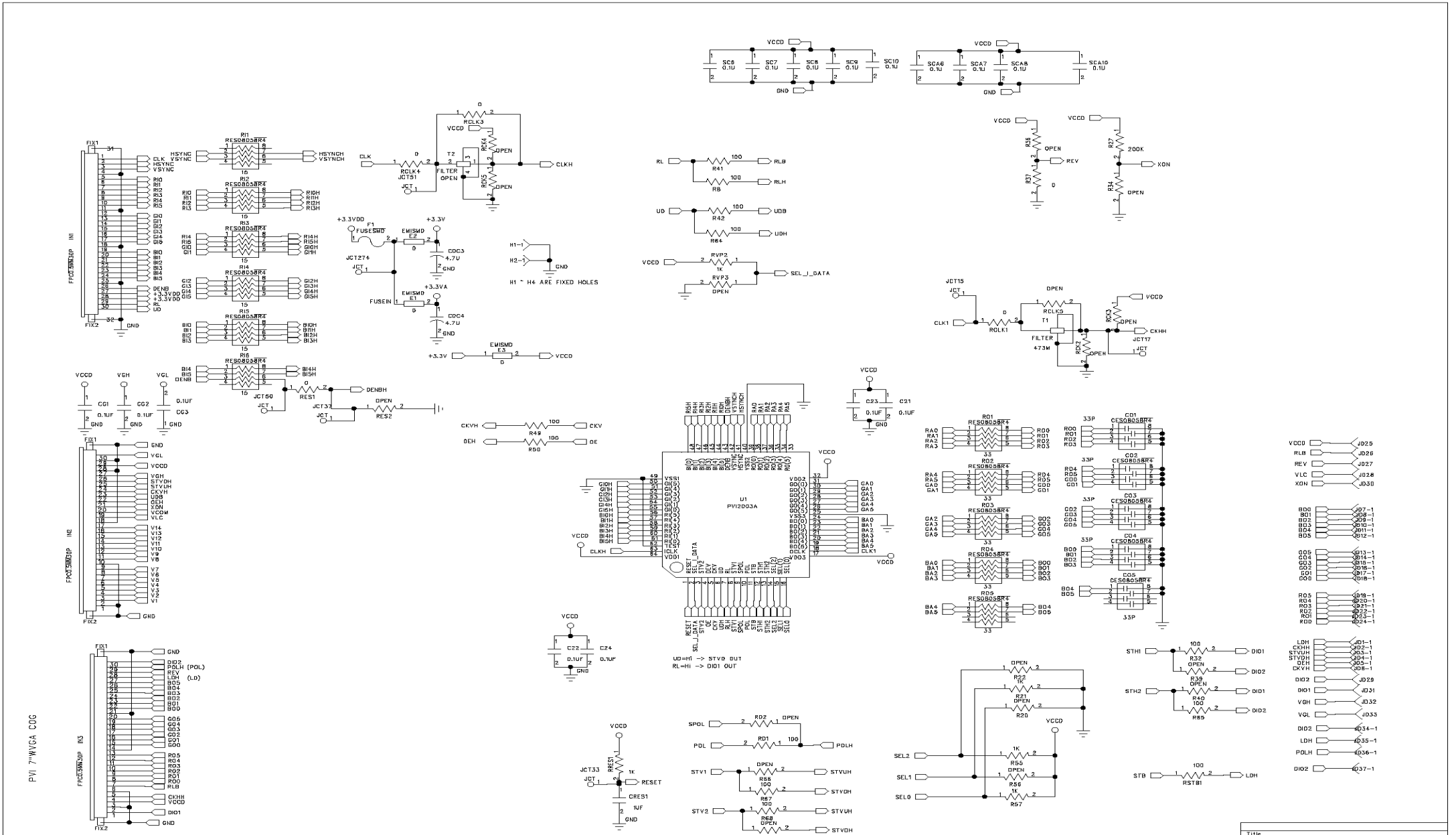


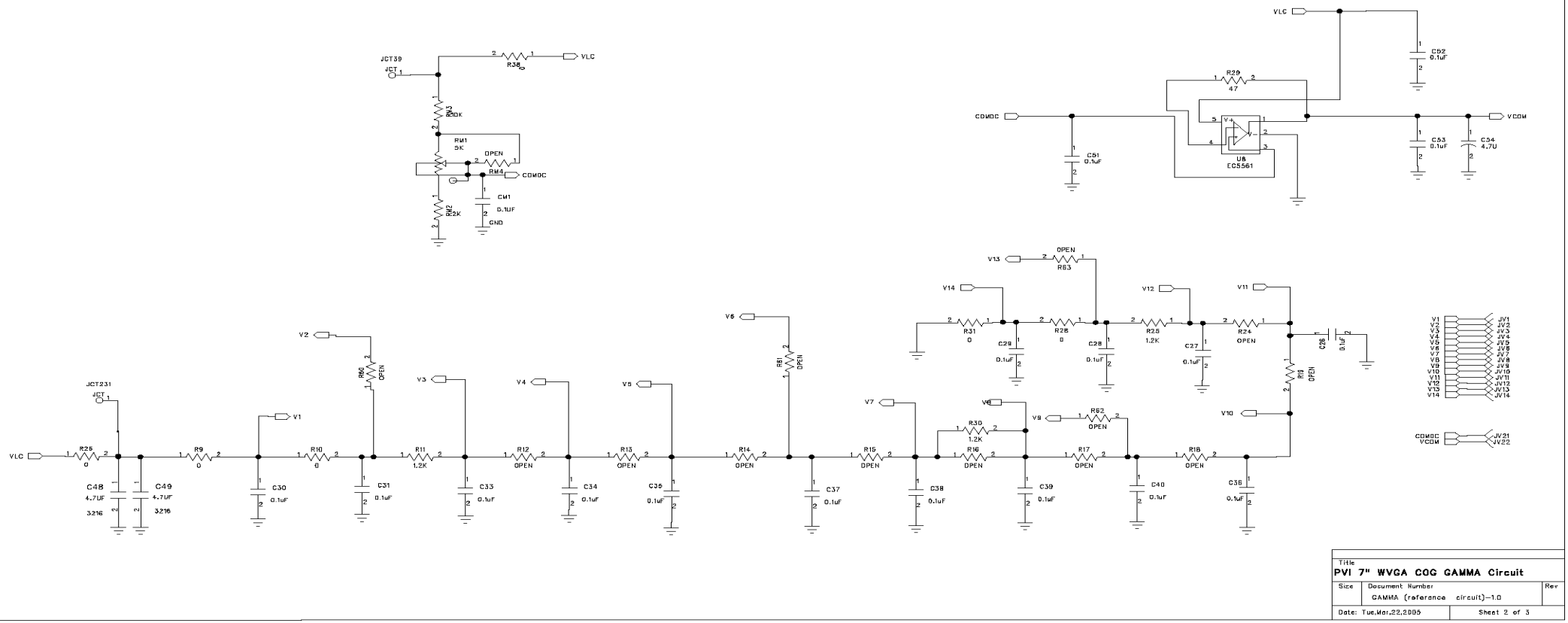
Title	PVI 10.2" WVGA COG GAMMA Circuit	
Size	Document Number: GAMMA (reference circuit)-1.0	Rev
Date: Tue,Mar,22,2005	Sheet 2 of 3	



Title	PVI 10.2" WVGA COG POWER Circuit	
Size	Document Number: POWER DC-DC (reference circuit)-1.0	Rev
Date: Tue,Mar,22,2005	Sheet 3 of 3	

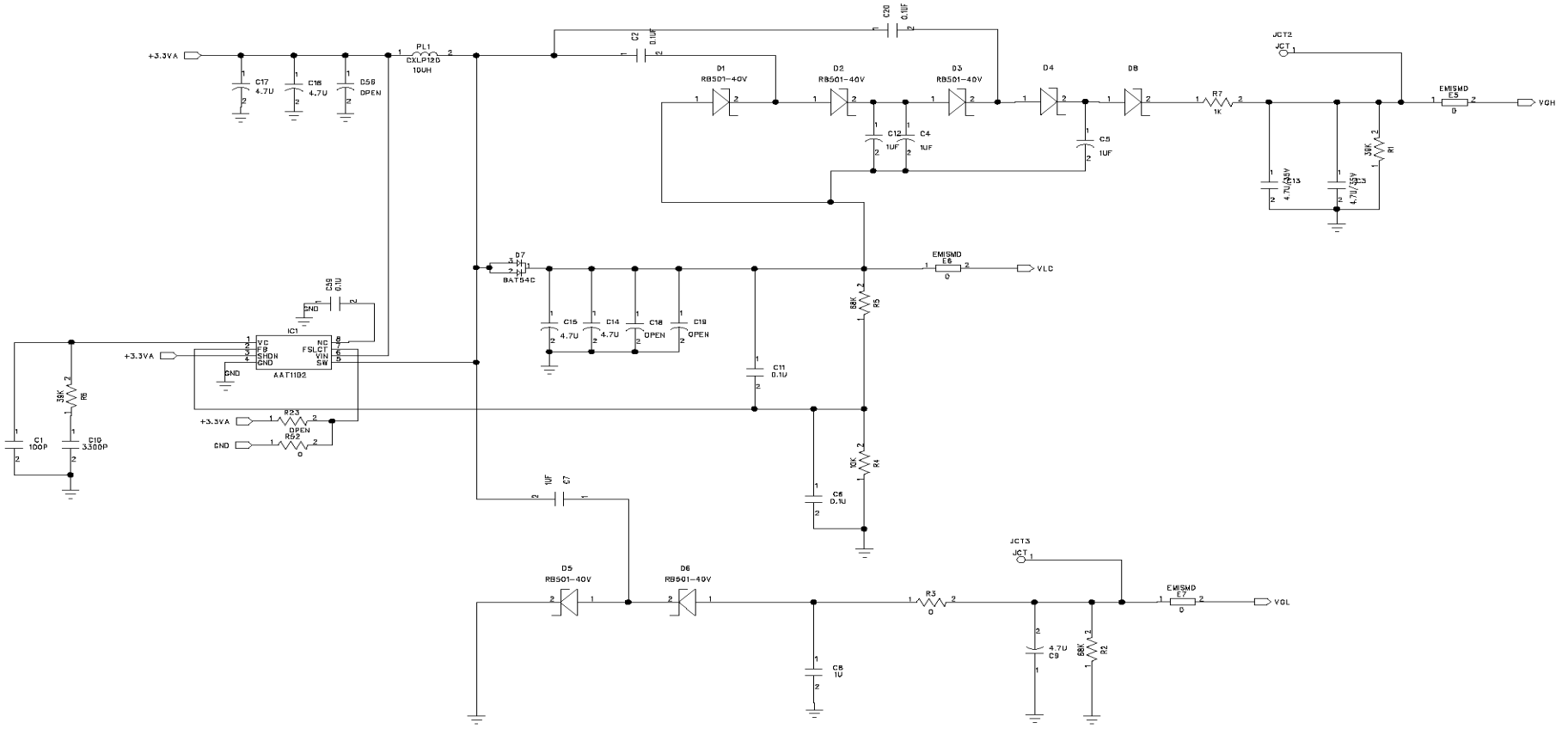
a.2 7 inch WVGA reference circuit in next three continuous pages.





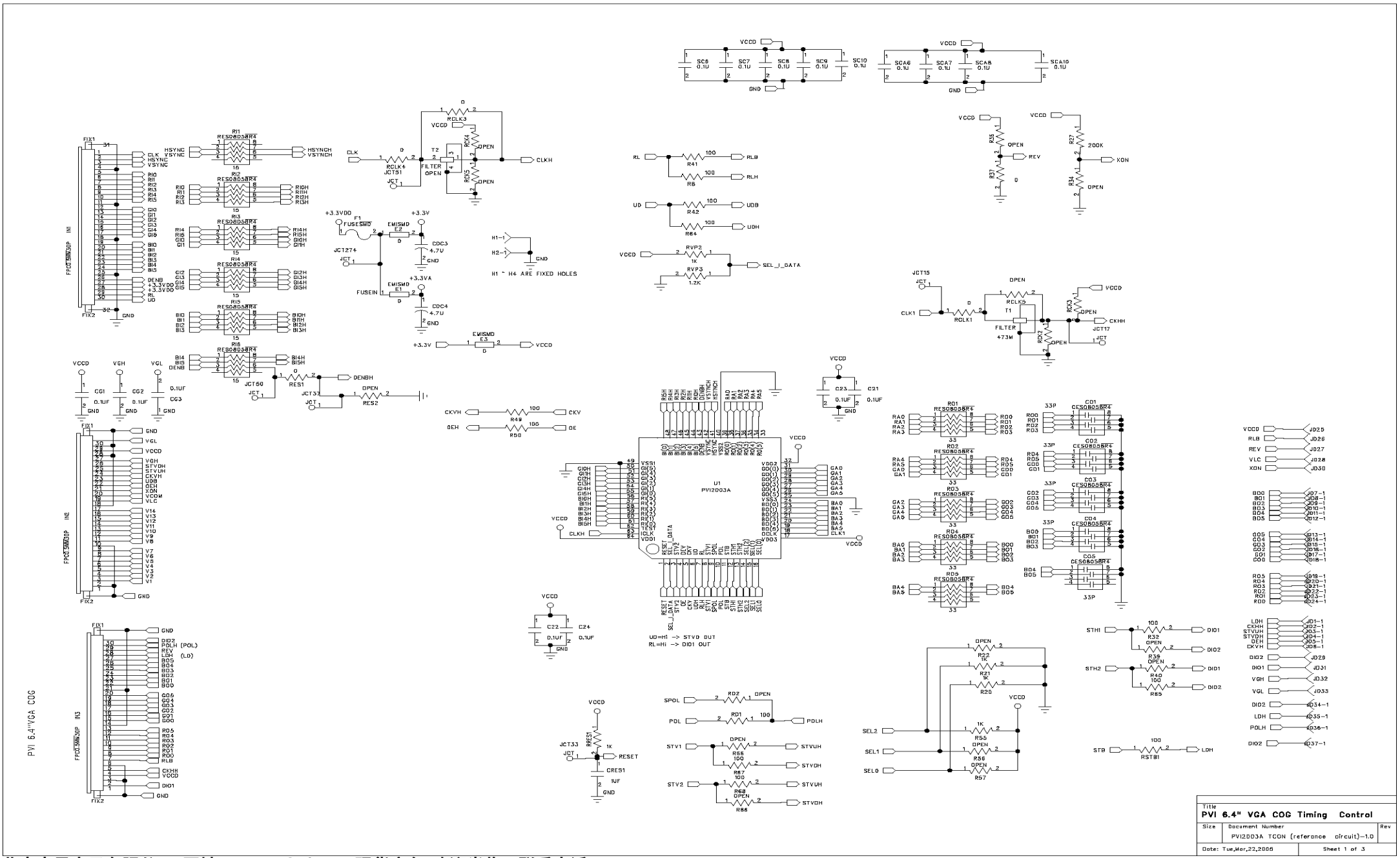
Title
PVI 7" WVGA COG GAMMA Circuit

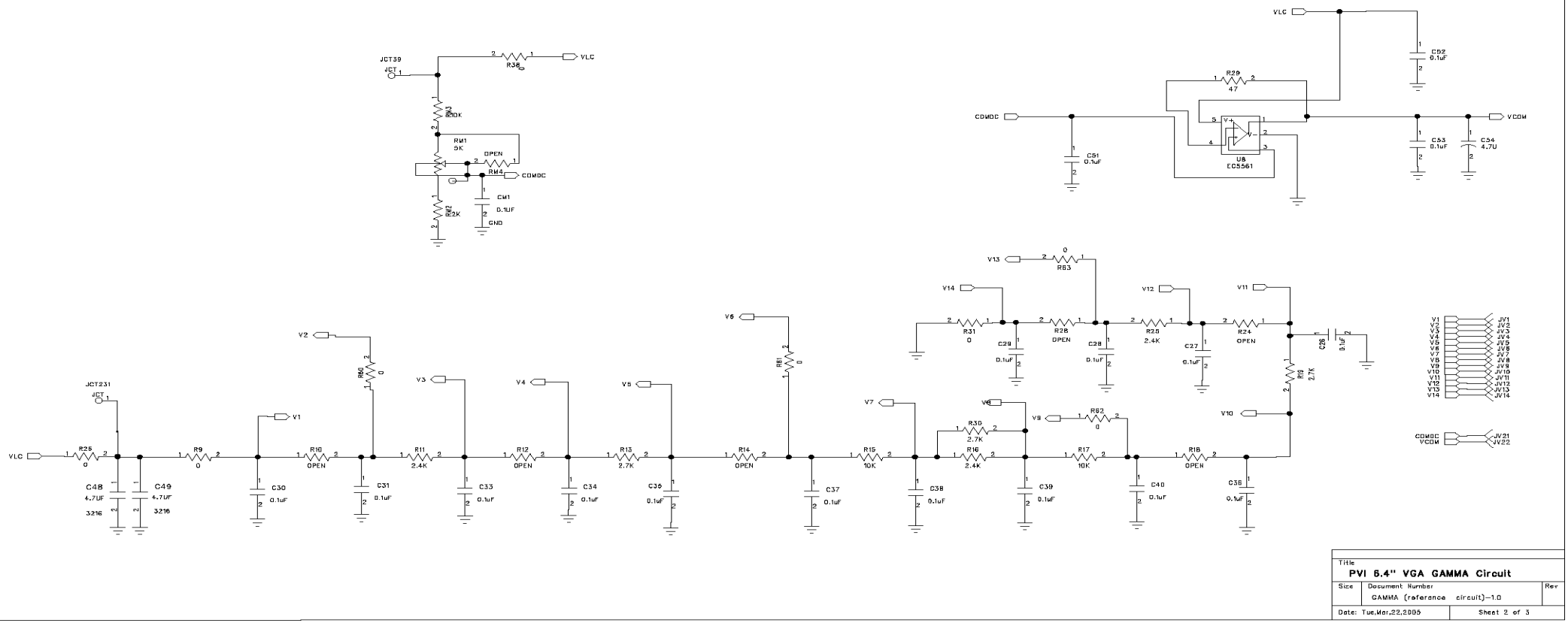
Size	Document Number	Rev
	GAMMA (reference circuit)-1.0	
Date: Tue,Mar,22,2005	Sheet 2 of 3	

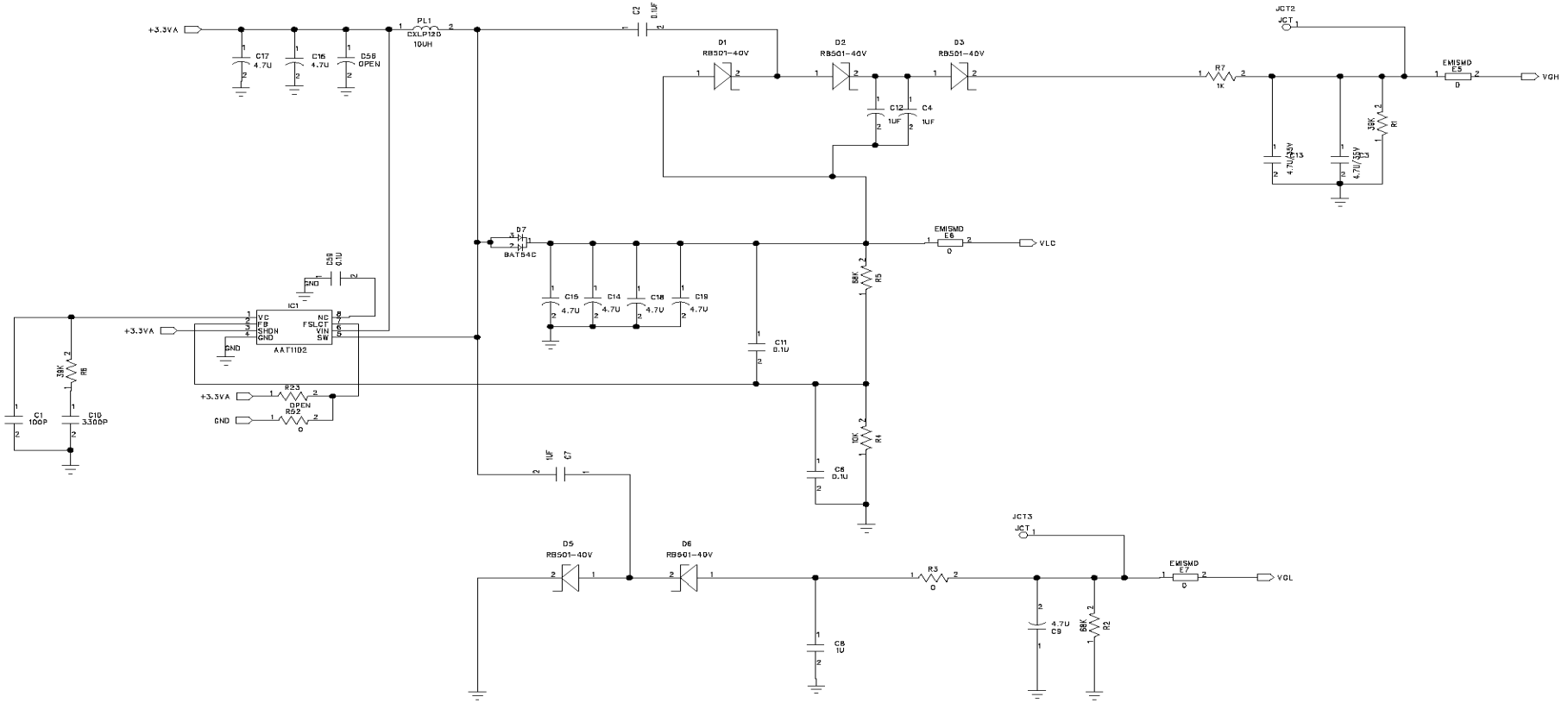


Title: PVI 7" WVGA COG POWER Circuit		
Size	Document Number: POWER DC-DC (reference circuit)-1.0	Rev
Date: Tue,Mar,22,2005	Sheet 3 of 3	

a.3 6.4 inch VGA reference circuit in next three continuous pages.





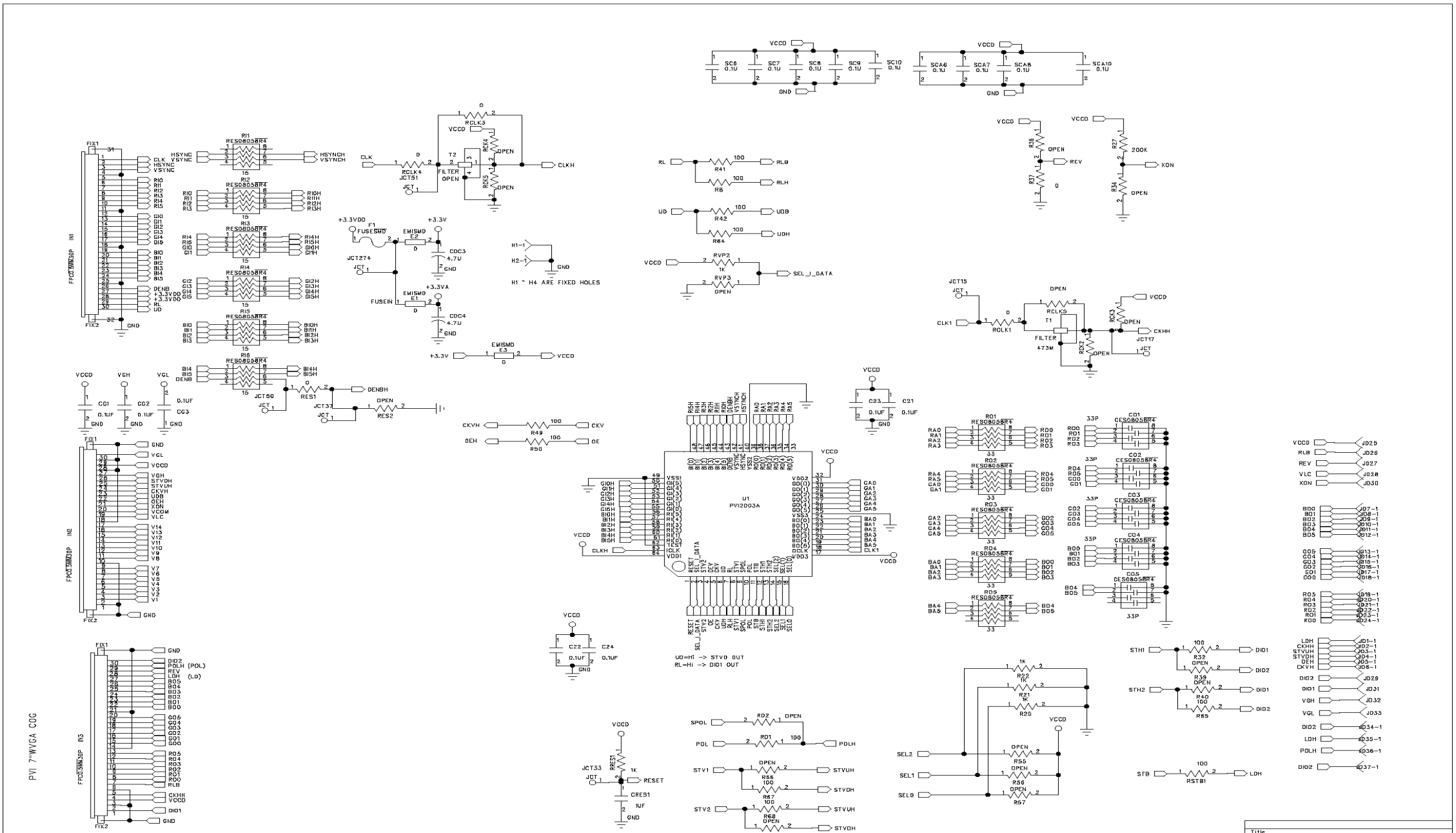


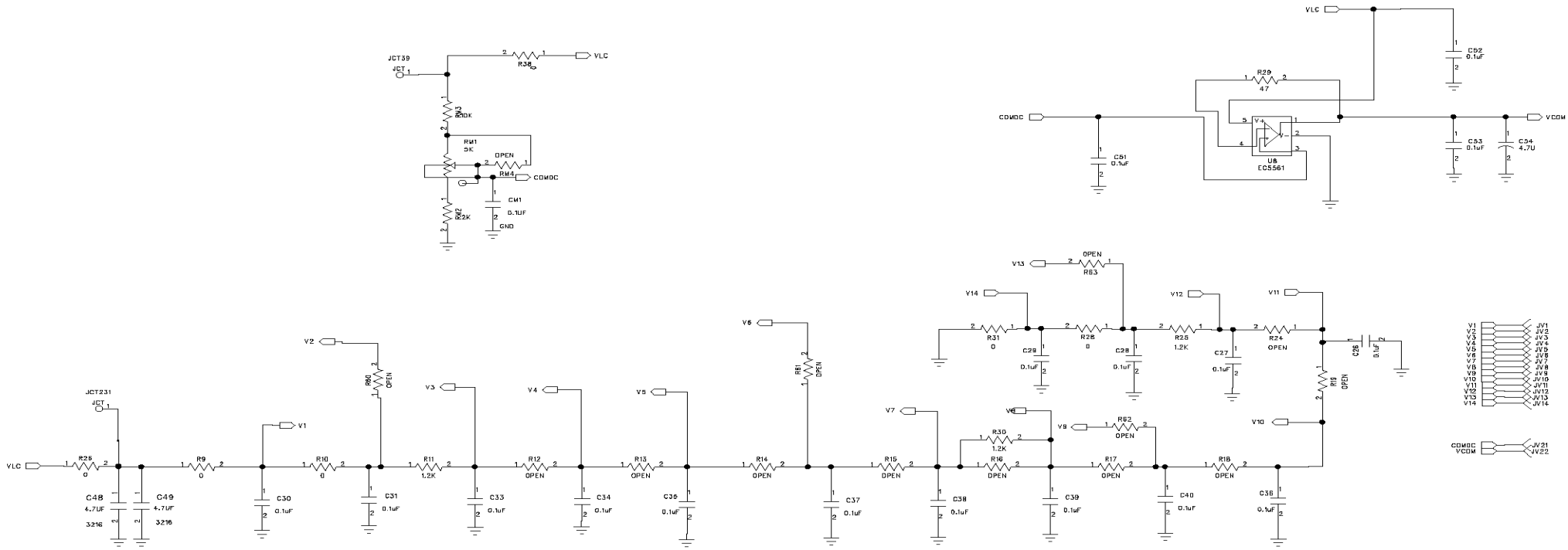
Title: PVI 6.4" VGA POWER Circuit

Size | Document Number: POWER DC-DC (reference circuit)-1.0 | Rev

Date: Tue,Mar,22,2005 | Sheet 3 of 3

a.4 4.2 inch 320*96 reference circuit in next three continuous pages.




VLC
R38
JCT39
R3
200K
RM1
5K
OPEN
RM4
COMDC
CM1
0.1UF
R2
22K
GND
C52
0.1uF
R29
47
C51
0.1uF
U6
EC5561
C53
0.1uF
C54
4.7U
VCOM
JCT231
R25
R9
R10
R11
1.2K
R12
R13
R14
R15
R16
R17
R18
R30
R31
R26
R25
R24
R19
R61
R62
R63
R66
C48
4.7UF
3216
C49
4.7UF
3216
C30
C31
C33
C34
C35
C36
C37
C38
C39
C40
C41
C26
C27
C28
C29
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
JV1
JV2
JV3
JV4
JV5
JV6
JV7
JV8
JV9
JV10
JV11
JV12
JV13
JV14
JV21
JV22
Title
PVI 4.2" 320*96 COG GAMMA Circuit
Size
Document Number
GAMMA (reference circuit)-1.0
Rev
Date: Tue,Mar,22,2005
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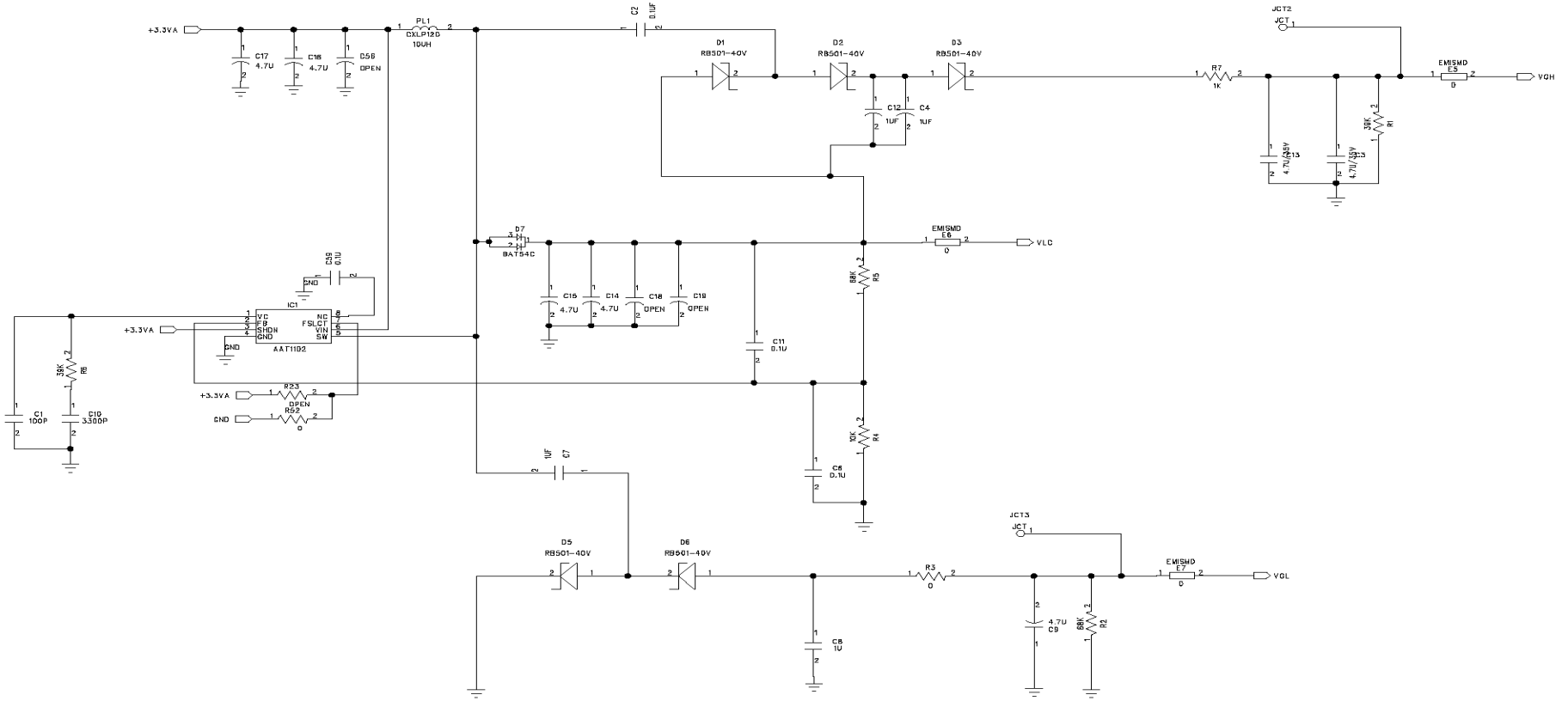

Title: PVI 4.2" 320*96 COG POWER Circuit		
Size	Document Number: POWER DC-DC (reference circuit)-1.0	Rev
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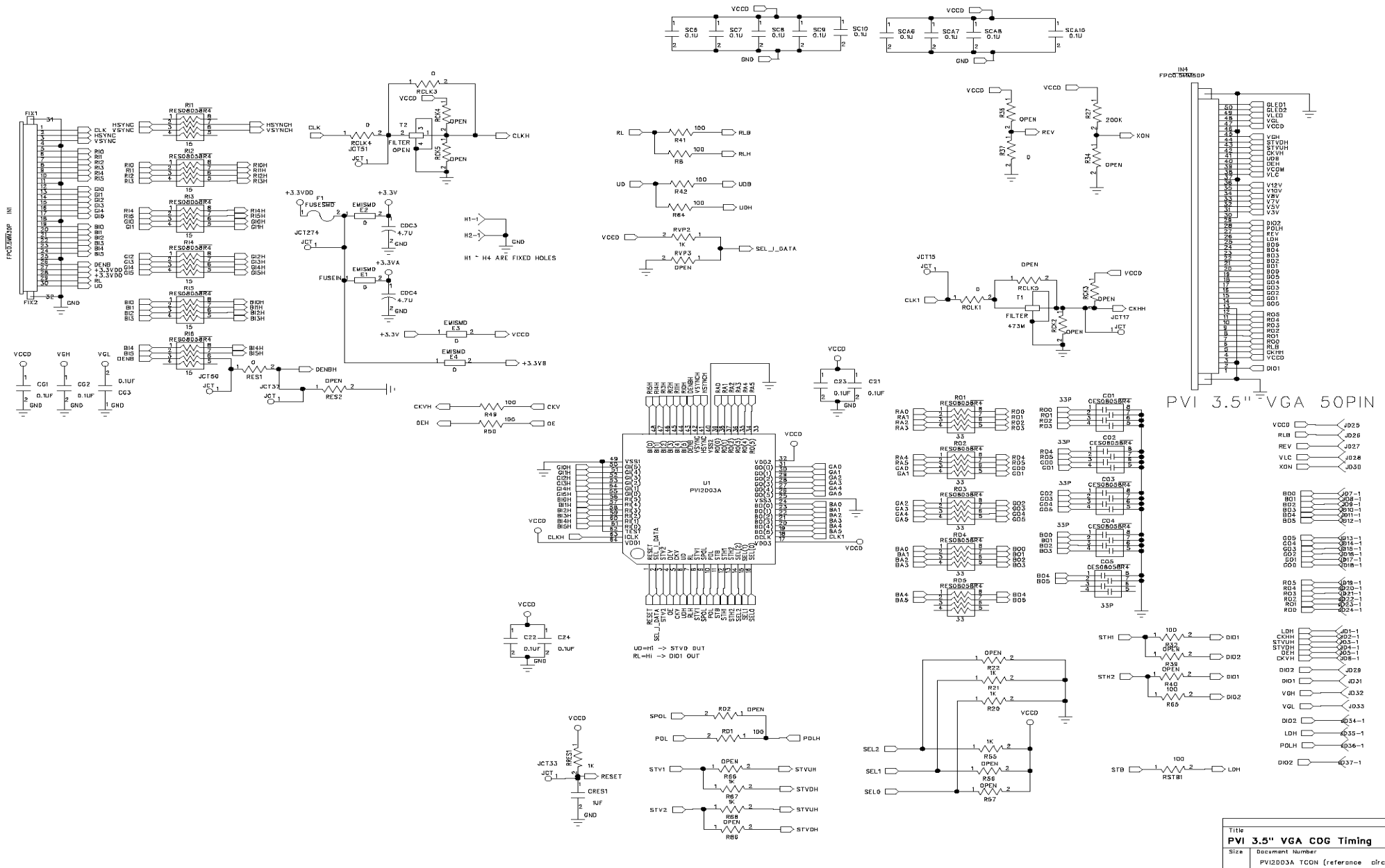
a.5 3.5 inch VGA reference circuit in next four continuous pages.


PVI 3.5" VGA 50PIN
U1
PVI2003A
UD=H1 -> STV0 OUT
RL=H1 -> DIO1 OUT
H1 ~ H4 ARE FIXED HOLES
Title
PVI 3.5" VGA COG Timing Control
Size
Document Number
PVI2003A TCON (reference circuit)-1.0
Rev
Date: Tue,Mar,22,2006
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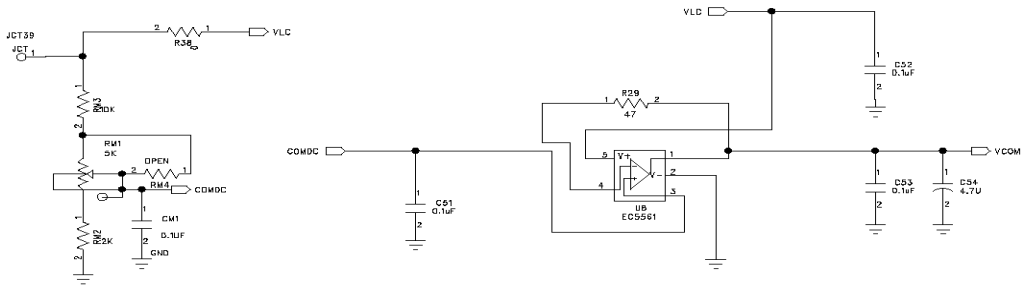

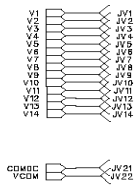

Title: PVI 3.5" VGA COG GAMMA Circuit		
Size	Document Number: VCOM (reference circuit)-1.0	Rev
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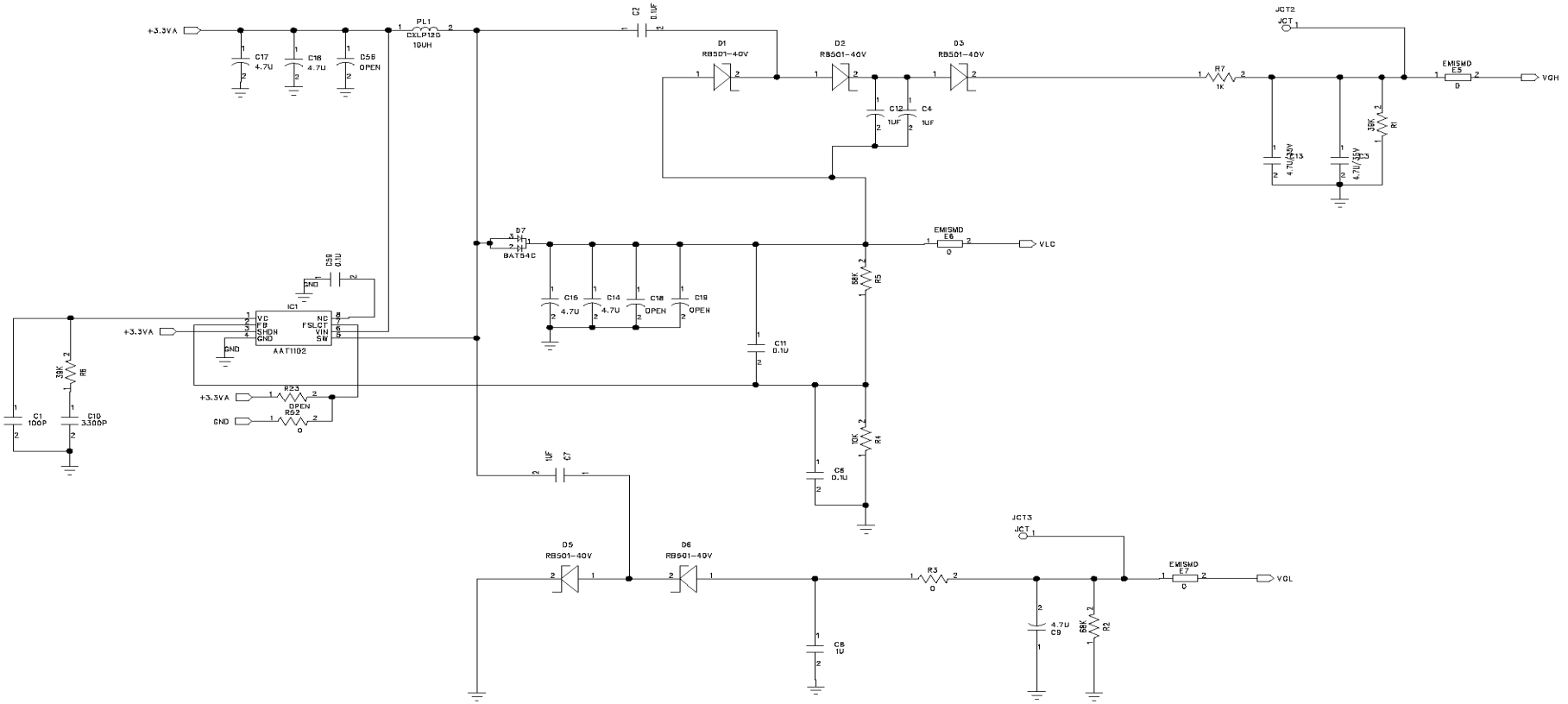

Title: PVI 3.5" VGA COG POWER Circuit		
Size	Document Number: POWER DC-DC (reference circuit)-1.0	Rev
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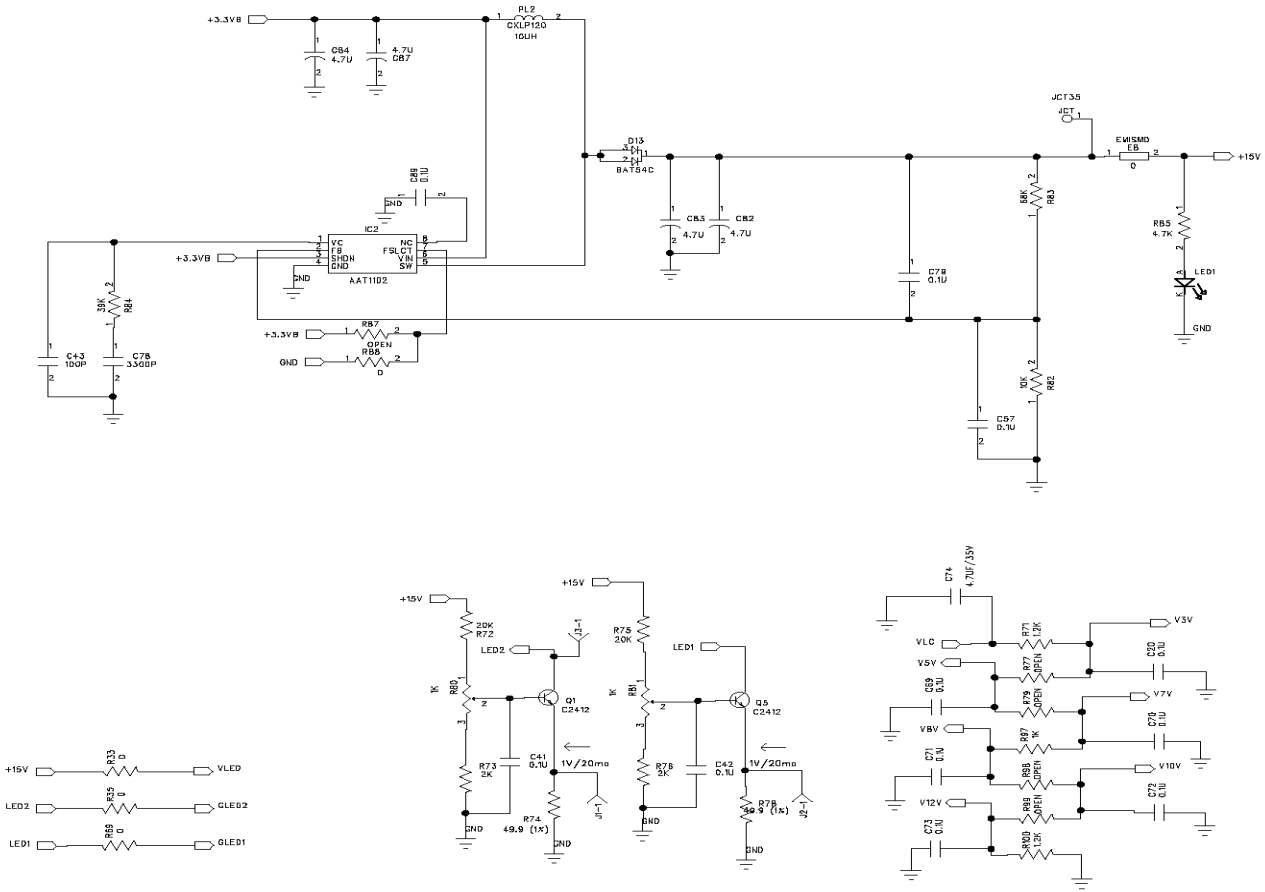

Title	PVI 3.5" VGA COG Gamma&LED circuit	
Size	Document number: Gamma&LED circuit(Referance circuit)—1.0	Rev
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Revision History

Rev.	Issued Date	Revised Contents
0.1	Mar/24/2005	New