Version : 1.2

TFT-LCD CONTROLLER LSI(PVI-2002A)

SPECIFICATION

MODEL NAME. : PVI-2002A

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By _____

Prepared By _____

PRIME VIEW INTERNATIONAL CO.,LTD.

3,LI SHIN RD. 1,SCIENCE-BASED

INDUSTRIAL PARK ,HSINCHU,TAIWAN,R.O.C.

Date : DEC /17/2004

Content:

1. General description

The PVI-2002A is timing controller IC to control PVI OA type TFT LCD modules. This IC generates all kind of control timing signals to the LCD source drivers and gate drivers. Also this IC provides different display mode.

2. Feature

*Support OA video system.
*Support multiple resolution mode(HVGA,VGA-350,VGA-400,VGA,SVGA).
*Support single/dual port RGB driver IC.
*Support DENB/SYNC mode auto-detect.
*provide timing scan for left/right and up/down shift control.
*dot inversion driving method.
*Package:TQFP-100pin(0.5mm pitch).
*single power supplies:+3.3V
*0.35u CMOS process,3.3V for core ,3.3/5V for input PAD and 3.3V for output PAD.

3. Pin assignment

Pin no.	Pin name	I/O	Remark	Pin No.	Pin name	I/O	Remark
1	VDD	I	3.3V	51	VDD	I	3.3V
2	HP[3]	I	Pull up	52	BO[5]	O	6mA
3	HP[2]	I	Pull down	53	BO[4]	O	6mA
4	HP[1]	I	Pull down	54	BO[3]	O	6mA
5	HP[0]	I	Pull down	55	BO[2]	O	6mA
6	VP[2]	I	Pull up	56	BO[1]	O	6mA
7	VP[1]	I	Pull down	57	BO[0]	O	6mA
8	VP[0]	I	Pull down	58	VSS	I	Ground
9	STV2	O	3-state(2mA)	59	GO[5]	O	6mA
10	VSS	I	Ground	60	GO[4]	O	6mA
11	OEV	O	2mA	61	GO[3]	O	6mA
12	CKV	O	2mA	62	GO[2]	O	6mA
13	UD	I		63	GO[1]	O	6mA
14	RL	I		64	GO[0]	O	6mA
15	STV1	O	3-state(2mA)	65	VSS	I	Ground
16	SPOL	O	2mA	66	RO[5]	O	6mA
17	POL	O	2mA	67	RO[4]	O	6mA
18	STB	O	2mA	68	RO[3]	O	6mA
19	STH1	O	3-state(2mA)	69	RO[2]	O	6mA
20	STH2	O	3-state(2mA)	70	RO[1]	O	6mA
21	SEL_STH	I		71	RO[0]	O	6mA
22	SEL[2]	I		72	HSYNC	I	
23	SEL[1]	I		73	VSYNC	I	
24	SEL[0]	I		74	DENB	I	
25	VDD	I	3.3V	75	VDD	I	3.3V
26	CKH1	O	6mA	76	VDD	I	3.3V
27	CKH3	O	6mA	77	BI[5]	I	
28	CKH2	O	6mA	78	BI[4]	I	
29	CKH4	O	6mA	79	BI[3]	I	
30	BO[11]	O	6mA	80	BI[2]	I	
31	BO[10]	O	6mA	81	BI[1]	I	
32	BO[9]	O	6mA	82	BI[0]	I	
33	BO[8]	O	6mA	83	VSS	I	Ground
34	BO[7]	O	6mA	84	GI[5]	I	
35	BO[6]	O	6mA	85	GI[4]	I	
36	VSS	I	Ground	86	GI[3]	I	
37	GO[11]	O	6mA	87	GI[2]	I	
38	GO[10]	O	6mA	88	GI[1]	I	
39	GO[9]	O	6mA	89	GI[0]	I	
40	GO[8]	O	6mA	90	VSS	I	Ground
41	GO[7]	O	6mA	91	RI[5]	I	
42	GO[6]	O	6mA	92	RI[4]	I	
43	VSS	I	Ground	93	RI[3]	I	
44	RO[11]	O	6mA	94	RI[2]	I	
45	RO[10]	O	6mA	95	RI[1]	I	
46	RO[9]	O	6mA	96	RI[0]	I	
47	RO[8	O	6mA	97	TEST	I	
48	RO[7]	O	6mA	98	ICLK	I	
49	RO[6]	O	6mA	99	RST	I	Schmitt
50	VDD	I	3.3V	100	SEL_I_DATA	I	

4. Pin description

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>VDD</td><td>I</td><td>Power 3.3V</td><td></td></tr>
<tr><td>2
3
4
5</td><td>HP[3]
HP[2]
HP[1]
HP[0]</td><td>I
I
I
I</td><td>Select horizontal start point(only if ASIC is set in SYNC mode)
<table>
<tr><th>HP[3]</th><th>HP[2]</th><th>HP[1]</th><th>HP[0]</th><th>Start point</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>Typ.-8</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>Typ.-7</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>Typ.-6</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>Typ.-5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>Typ.-4</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>Typ.-3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>Typ.-2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>Typ.-1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>Typ.+0</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>Typ.+1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>Typ.+2</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>Typ.+3</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>Typ.+4</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>Typ.+5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>L</td><td>Typ.+6</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>Typ.+7</td></tr>
</table></td><td>Note 1</td></tr>
<tr><td>6
7
8</td><td>VP[2]
VP[1]
VP[0]</td><td>I
I
I</td><td>Select vertical start line (only if ASIC is set in SYNC mode)
<table>
<tr><th>VP[2]</th><th>VP[1]</th><th>VP[0]</th><th>Start line</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Typ.-4</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Typ.-3</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Typ.-2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Typ.-1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Typ.+0</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Typ.+1</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Typ.+2</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Typ.+3</td></tr>
</table></td><td>Note1</td></tr>
<tr><td>9</td><td>STV2</td><td>O</td><td>Gate driver start pulse
1. UD=L: STV2 is output pin of start pulse.
2. UD=H: STV2 is in high impedance state.</td><td>Note 2</td></tr>
<tr><td>10</td><td>VSS</td><td>I</td><td>Ground</td><td></td></tr>
<tr><td>11</td><td>OEV</td><td>O</td><td>Output enable control signal for gate driver
OEV=H : gate driver output equal VEE.</td><td></td></tr>
<tr><td>12</td><td>CKV</td><td>O</td><td>Gate driver shift clock</td><td></td></tr>
<tr><td>13</td><td>UD</td><td>I</td><td>Select up/down direction
1.UD=H : normal scan.
2.UD=L : reverse scan.</td><td>Note 2</td></tr>
<tr><td>14</td><td>RL</td><td>I</td><td>Select left/right direction</td><td>Note3</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>1.RL=H : normal scan.
2.RL=L : reverse scan.</td><td></td></tr>
<tr><td>15</td><td>STV1</td><td>O</td><td>Gate driver start pulse
1.UD=H: STV1 is output pin of start pulse.
2.UD=L: STV1 is in high impedance state.</td><td>Note 2</td></tr>
<tr><td>16</td><td>SPOL</td><td>O</td><td>Source driver 2-line polarity inverting.</td><td>Note 4</td></tr>
<tr><td>17</td><td>POL</td><td>O</td><td>Source driver line polarity inverting.</td><td>Note 4</td></tr>
<tr><td>18</td><td>STB</td><td>O</td><td>Source driver latch pulse(high active).</td><td></td></tr>
<tr><td>19</td><td>STH1</td><td>O</td><td>Source driver start pulse
1.RL=H : STH1 is output pin of start pulse.
2.RL=L : STH1 is in high impedance state.</td><td>Note 3</td></tr>
<tr><td>20</td><td>STH2</td><td>O</td><td>Source driver start pulse
1.RL=L : STH2 is output pin of start pulse.
2.RL=H : STH2 is in high impedance state.</td><td>Note 3</td></tr>
<tr><td>21</td><td>SEL_STH</td><td>I</td><td>Select STH1/STH2 output start pulse for short/long time.
1.SEL_STH=H : STH1/STH2 output start pulse for long time.
2.SEL_STH=L : STH1/STH2 output start pulse for short time.</td><td></td></tr>
<tr><td>22
23
24</td><td>SEL[2]
SEL[1]
SEL[0]</td><td>I
I
I</td><td>Select display mode
<table>
<tr><th>SEL[2]</th><th>SEL[1]</th><th>SEL[0]</th><th>Display</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>SVGA(RGB dual port)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>VGA-350,VGA-400,VGA (RGB dual port)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>SVGA(RGB dual port)</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>SVGA(RGB single port)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>VGA-350,VGA-400,VGA (RGB single port)</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>WVGA(RGB single port)</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>HVGA*1(RGB single port)</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>HVGA*2(RGB single port)</td></tr>
</table></td><td>Note 4
Note 6</td></tr>
<tr><td>25</td><td>VDD</td><td>I</td><td>Power 3.3V</td><td></td></tr>
<tr><td>26
27
28
29</td><td>CKH1
CKH3
CKH2
CKH4</td><td>O
O
O
O</td><td>Source driver shift clock</td><td>Note 5</td></tr>
<tr><td>30
31
32
33
34
35</td><td>BO[11]
BO[10]
BO[9]
BO[8]
BO[7]
BO[6]</td><td>O
O
O
O
O
O</td><td>Blue color(dual/single port)</td><td>Note 6</td></tr>
<tr><td>36</td><td>VSS</td><td>I</td><td>Ground</td><td></td></tr>
<tr><td>37
38
39
40
41</td><td>GO[11]
GO[10]
GO[9]
GO[8]
GO[7]</td><td>O
O
O
O
O</td><td>Green color (dual/single port)</td><td>Note 6</td></tr>
</table>

42	GO[6]	O		
43	VSS	I	Ground	
44	RO[11]	O	Red color(dual/single port)	Note 6
45	RO[10]	O		
46	RO[9]	O		
47	RO[8]	O		
48	RO[7]	O	Red color(dual/single port)	Note 6
49	RO[6]	O		
50	VDD	I	Power 3.3V	
51	VDD	I	Power 3.3V	
52	BO[5]	O	Blue color(dual port)	Note 6
53	BO[4]	O		
54	BO[3]	O		
55	BO[2]	O		
56	BO[1]	O		
57	BO[0]	O		
58	VSS	I	Ground	
59	GO[5]	O	Green color(dual port)	Note 6
60	GO[4]	O		
61	GO[3]	O		
62	GO[2]	O		
63	GO[1]	O		
64	GO[0]	O		
65	VSS	I	Ground	
66	RO[5]	O	Red color(dual port)	Note 6
67	RO[4]	O		
68	RO[3]	O		
69	RO[2]	O		
70	RO[1]	O		
71	RO[0]	O		
72	HSYNC	I	Horizontal sync signal in SYNC mode	Note 1
73	VSYNC	I	Vertical sync signal in SYNC mode	Note 1
74	DENB	I	Data enable signal in DENB mode	Note 1
75	VDD	I	Power 3.3V	
76	VDD	I	Power 3.3V	
77	BI[5]	I	Blue color	Note 7
78	BI[4]	I		
79	BI[3]	I		
80	BI[2]	I		
81	BI[1]	I		
82	BI[0]	I		
83	VSS	I	Ground	
84	GI[5]	I	Green color	Note 7
85	GI[4]	I		
86	GI[3]	I		
87	GI[2]	I		
88	GI[1]	I		
89	GI[0]	I		
90	VSS	I	Ground	
91	RI[5]	I	Red color	Note 7
92	RI[4]	I		
93	RI[3]	I		

94 95 96	RI[2] RI[1] RI[0]	I I I		
97	TEST	I	Select AC/DC test TEST=H : AC/DC test mode. TEST=L : normal mode.	
98	ICLK	I	System clock	
99	RST	I	Reset pin in ASIC 1.RST=H : normal state. 2.RST=L : reset state.	
100	SEL_I_DATA	I	Select RI,GI,BI data conversion 1.SEL_I_DATA=L : normal RI,GI,BI data 2.SEL_I_DATA=H : reverse RI,GI,BI data	Note 7

Note 1: if ASIC is set in SYNC(HSYNC+VSYNC)mode, DENB pin have to be always hold high or low voltage.

When ASIC's DENB pin receive AC toggle signal, then ASIC is set in DENB mode.

Note 2: UD control gate driver up/down direction

1.UD=H : STV1 →G1→G2→G3→G4→G5→G6→G7→G8→------→STV2

2.UD=L : STV1 ←G1←G2←G3←G4←G5←G6←G7←G8←----- ←STV2

Note 3: RL control source driver right/left direction

1.RL=H : STH1→S1→S2→S3→S4→S5→S6→S7→S8→------→STH2

2.RL=L : STH1←S1←S2←S3←S4←S5←S6←S7←S8←------←STH2

Note 4:

SVGA	800*600 panel resolution
WVGA	800*480 panel resolution
VGA	640*480 panel resolution
VGA-350(SYNC mode)	640*480 panel resolution
VGA-400(SYNC mode)	640*480 panel resolution
HVGA	640*240 panel resolution

When ASIC use VGA-350 or VGA-400 mode, then SPOL become POL.

SYNC mode	HSYNC polarity	VSYNC polarity
VGA-350	Positive	Negative
VGA-400	Negative	Positive
VGA	Positive Negative	Positive Negative
SVGA WVGA HVGA	Negative Negative Negative	Negative Negative Negative

Note 5: source driver shift clock

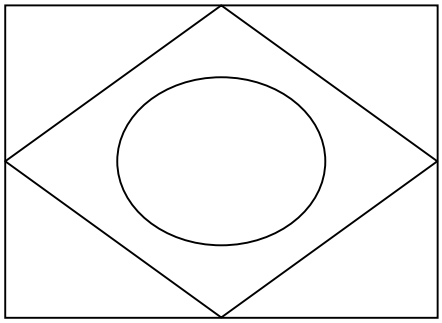
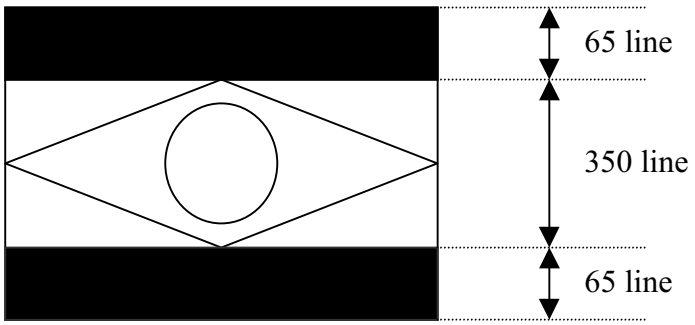
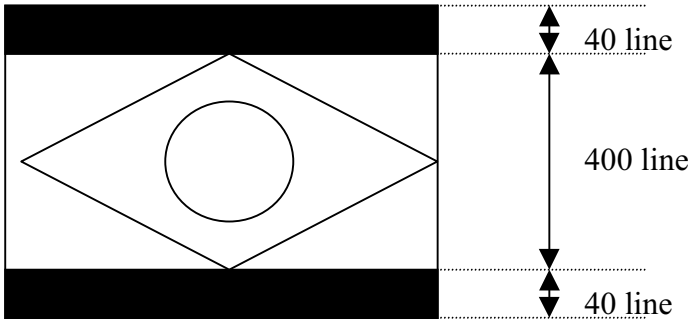
CKH1=CKH2 for RGB dual port driver.

CKH3=CKH4 for RGB single port driver.

Note 6: When ASIC use output RGB single port, then RO[5..0]=000000,GO[5..0] =000000
And BO[5..0]=000000

Note 7: select RI,GI,BI data conversion
1.SEL_I_DATA=H:
RI[5..0] become BI[0..5]
GI[5..0] become GI[0..5]
BI[5..0] become RI[0..5]

5. Display mode

Display mode	Display characteristic
SVGA(full screen) WVGA(full screen) VGA(full screen) HVGA(full screen)	
VGA-350	
VGA-400	

6. Electrical characteristic

6.1 Absolute maximum rating

Parameter	Symbol	limit	Unit	Remark
Power supply voltage	VDD	VSS-0.3 to 4.0	V	
Input voltage	Vin	VSS-0.3 to 7.0	V	
Output voltage	Vout	VSS-0.3 to VDD+0.5	V	
Storage temperature	Tstg	-65 to 150	℃	

6.2 Recommended operating condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage	VDD	3.0	3.3	3.6	V	
Input voltage	Vin	0	-	5.5	V	
Operating temperature	Toper	-40	-	85	℃	

6.3 General DC characteristic

Parameter	Symbol	condition	Min.	Typ.	Max.	Unit	Remark
Input leakage current	I_{LC}	VDD=max V_{IH}=VDD V_{IL}=0V	-1	-	1	uA	
Logic input low voltage	V_{IL}	VDD=min	-	-	0.8	V	
Logic input high voltage	V_{IH}	VDD=max	2.0	-	-	V	
Schmitt input low voltage	V_{SIL}	VDD=min	0.6	-	1.8	V	
Schmitt input high voltage	V_{SIH}	VDD=max	1.1	-	2.4	V	
Output low voltage	V_{OL}	VDD=min	VSS-0.4	-	-	V	
Output high voltage	V_{OH}	VDD=max	-	-	VDD+0.4	V	
Input pull up/down resistance	R_I	V_{IL}=0V or V_{IH}=VDD	-	50	-	kΩ	

7. Timing condition(reference A. The timing diagram in page 35)

7.1 SVGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	40	-	MHz	
		tc	-	25	-	ns	
HSYNC	Period	Hp	-	26.4	-	us	
			-	1056	-	tc	
	Display period	Hdp	-	800	-	tc	
	Pulse width	Hpw	12	128	135	tc	
	Back-porch	Hbp	86	86	209	tc	
	Front-porch	Hfp	-	42	-	tc	
	Hpw+Hbp		206	214	221	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.579	-	ms	
			624	628	800	Hp	
	Display period	Vdp	-	600	-	Hp	
	Pulse width	Vpw	2	4	25	Hp	
	Back-porch	Vbp	2	23	25	Hp	
	Front-porch	Vfp	1	1	-	Hp	
	Vpw+Vbp		23	27	30	Hp	
DENB	Horizontal scanning period	T1	860	1056	1064	tc	
	Horizontal display period	T2	-	800	-	tc	
	Vertical display period	T3	-	600	-	T1	
	Frame cycling period	T4	604	628	800		
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	25(50)	-	ns	
Tod	25(50)	-	-	ns	
Tsth_1	-	25(50)	-	ns	
Tsth_2	-	20	-	us	
Tstb	-	2	-	us	
Tpol	-	26.4	-	us	
Tspol	-	52.8	-	us	
Tstv	-	28.5	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.2 WVGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	32	-	MHz	
		tc	-	31.25	-	ns	
HSYNC	Period	Hp	-	33	-	us	
			-	1056	-	tc	
	Display period	Hdp	-	800	-	tc	
	Pulse width	Hpw	12	128	13	tc	
	Back-porch	Hbp	86	86	209	tc	
	Front-porch	Hfp	-	42	-	tc	
	Hpw+Hbp		206	214	221	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	17.325	-	ms	
			515	525	800	Hp	
	Display period	Vdp	-	480	-	Hp	
	Pulse width	Vpw	2	2	35	Hp	
	Back-porch	Vbp	2	33	35	Hp	
	Front-porch	Vfp	1	10	-	Hp	
	Vpw+Vbp		31	35	38	Hp	
DENB	Horizontal scanning period	T1	860	1056	1064	tc	
	Horizontal display period	T2	-	800	-	tc	
	Vertical display period	T3	-	480	-	T1	
	Frame cycling period	T4	520	525	800		
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	31.25(62.5)	-	ns	
Tod	31.25(62.5)	-	-	ns	
Tsth_1	-	31.25(62.5)	-	ns	
Tsth_2	-	25	-	us	
Tstb	-	2.5	-	us	
Tpol	-	33	-	us	
Tspol	-	66	-	us	
Tstv	-	35.625	-	us	
Tckv	-	7.5	-	us	
Toev	-	6.25	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.3 VGA mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	12	96	139	tc	
	Back-porch	Hbp	12	48	139	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		136	144	151	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			515	525	800	Hp	
	Display period	Vdp	-	480	-	Hp	
	Pulse width	Vpw	2	2	35	Hp	
	Back-porch	Vbp	2	33	35	Hp	
	Front-porch	Vfp	1	10	-	Hp	
	Vpw+Vbp		31	35	38	Hp	
DENB	Horizontal scanning period	T1	780	800	900	tc	
	Horizontal display period	T2	-	640	-	tc	
	Vertical display period	T3	-	480	-	T1	
	Frame cycling period	T4	520	525	1024	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40(80)	-	ns	
Tod	40(80)	-	-	ns	
Tsth_1	-	40(80)	-	ns	
Tsth_2	-	25.6	-	us	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.4 VGA-350 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	12	96	139	tc	
	Back-porch	Hbp	12	48	139	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		136	144	151	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	14.3	-	ms	
			447	449	510	Hp	
	Display period	Vdp	-	350	-	Hp	
	Pulse width	Vpw	2	2	35	Hp	
	Back-porch	Vbp	2	60	63	Hp	
	Front-porch	Vfp	-	37	-	Hp	
	Vpw+Vbp		58	62	65	Hp	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40(80)	-	ns	
Tod	40(80)	-	-	ns	
Tsth_1	-	40(80)	-	ns	
Tsth_2	-	25.6	-	us	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.5 VGA-400 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	12	96	139	tc	
	Back-porch	Hbp	12	48	139	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		136	144	151	tc	Note 1
	Hsync-CLK	Hhc	10		Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	14.3	-	ms	
			446	449	480	Hp	
	Display period	Vdp	-	400	-	Hp	
	Pulse width	Vpw	2	2	35	Hp	
	Back-porch	Vbp	2	35	38	Hp	
	Front-porch	Vfp	-	12	-	Hp	
	Vpw+Vbp		33	37	40	Hp	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40(80)	-	ns	
Tod	40(80)	-	-	ns	
Tsth_1	-	40(80)	-	ns	
Tsth_2	-	25.6	-	us	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.6 HVGA*1 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	12.5	-	MHz	
		tc	-	80	-	ns	
HSYNC	Period	Hp	-	64	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	12	96	200	tc	
	Back-porch	Hbp	12	48	64	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		136	144	151	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			157	262	400	Hp	
	Display period	Vdp	-	240	-	Hp	
	Pulse width	Vpw	2	2	15	Hp	
	Back-porch	Vbp	2	15	15	Hp	
	Front-porch	Vfp	1	5	-	Hp	
	Vpw+Vbp		14	17	19	Hp	
DENB	Horizontal scanning period	T1	780	800	900	tc	
	Horizontal display period	T2	-	640	-	tc	
	Vertical display period	T3	-	240	-	T1	
	Frame cycling period	T4	157	262	400	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	80(160)	-	ns	
Tod	80(160)	-	-	ns	
Tsth_1	-	80(160)	-	ns	
Tsth_2	-	51.2	-	us	
Tstb	-	6.4	-	us	
Tpol	-	64	-	us	
Tspol	-	128	-	us	
Tstv	-	78.4	-	us	
Tckv	-	19.2	-	us	
Toev	-	16	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

7.7 HVGA*2 mode

a. Input signal characteristic

		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
ICLK	Frequency	1/tc	-	25.175	-	MHz	
		tc	-	40	-	ns	
HSYNC	Period	Hp	-	32	-	us	
			-	800	-	tc	
	Display period	Hdp	-	640	-	tc	
	Pulse width	Hpw	12	96	200	tc	
	Back-porch	Hbp	12	48	64	tc	
	Front-porch	Hfp	-	16	-	tc	
	Hpw+Hbp		136	144	151	tc	Note 1
	Hsync-CLK	Hhc	10	-	Tc-10	ns	
	Vsync-Hsync	Hvh	0	0	200	tc	
VSYNC	Period	Vp	-	16.8	-	ms	
			515	525	800	Hp	
	Display period	Vdp	-	240	-	Hp	
	Pulse width	Vpw	2	2	35	Hp	
	Back-porch	Vbp	2	33	35	Hp	
	Front-porch	Vfp	1	10	-	Hp	
	Vpw+Vbp		31	35	38	Hp	
DENB	Horizontal scanning period	T1	780	800	900	tc	
	Horizontal display period	T2	-	640	-	tc	
	Vertical display period	T3	-	240	-	T1	
	Frame cycling period	T4	515	525	800	T1	
RI,GI,BI	CLK-DATA	Dcd	10	-	-	ns	
	DATA-CLK	Ddc	8	-	-	ns	

b. Output signal characteristic

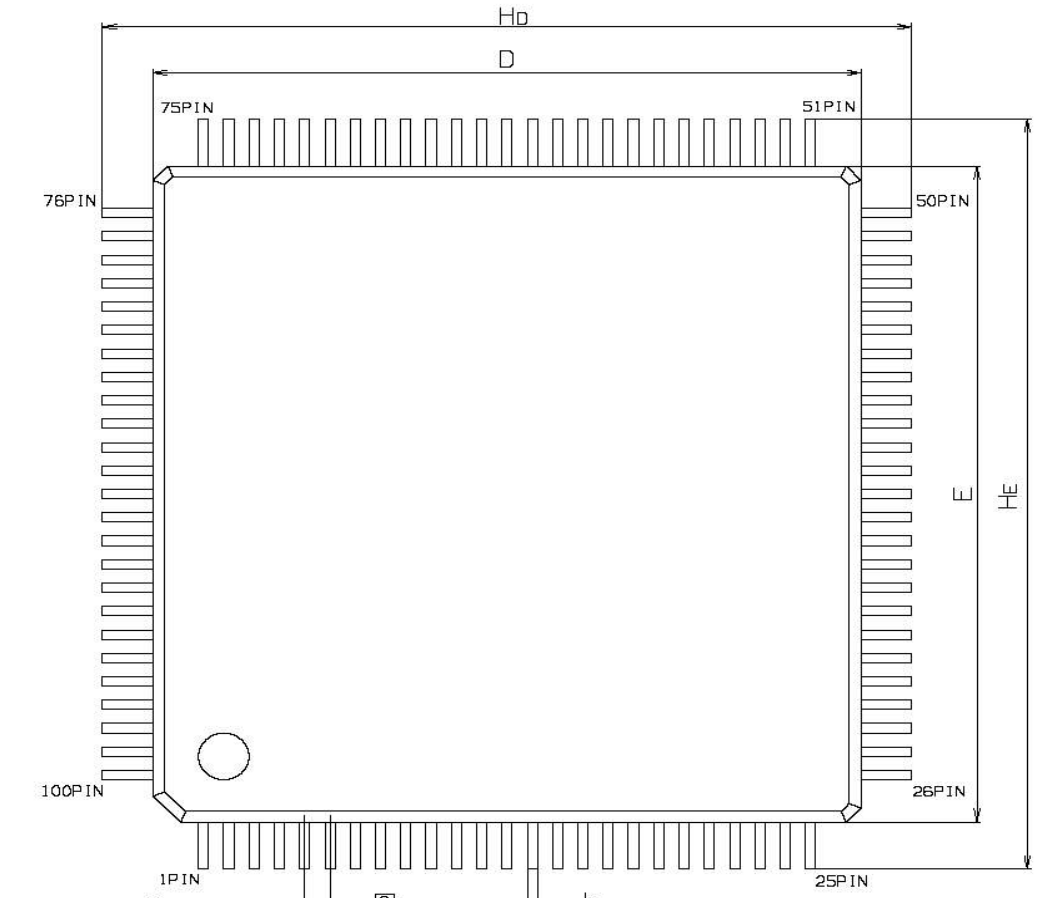
Symbol	Min.	Typ.	Max.	Unit	Remark
Toc	-	40(80)	-	ns	
Tod	40(80)	-	-	ns	
Tsth_1	-	40(80)	-	ns	
Tsth_2	-	25.6	-	us	
Tstb	-	3.2	-	us	
Tpol	-	32	-	us	
Tspol	-	64	-	us	
Tstv	-	39.2	-	us	
Tckv	-	6	-	us	
Toev	-	5	-	us	

Note: When ASIC use RGB dual port , then ( )'s value is right.

8. Reliability test item

No.	Test item	condition	remark
1	High temperature storage	Ta=150℃ 240h	
2	Low temperature storage	Ta=-60℃ 240h	
3	High temperature operation	Ta=85℃ 240h	
4	Low temperature operation	Ta=-40℃ 240h	
5	High temperature and High humidity	Ta=80℃ , 95%RH 240h	operation
6	Heat shock	-30℃, 25℃, 80℃ 200cycle 30min,5min,30min	Non-operation
7	Electrostatic discharge	± 200V,200pF(0Ω) once for each terminal	Non-operation

9. Package information



Symbol	Dimension in Milimeters		
	Min	Nom	Max
E	13.9	14	14.1
D	13.9	14	14.1
Amax			1.2
A_1		0.1	
A_2	0.9	1	1.1
e		0.5	
* b	0.13		0.27
* c	0.1	0.18	0.2
* b1	0.13	0.2	0.23
* c1	0.1	0.125	0.16
θ	0°		10°
L	0.3	0.5	0.7
L_1		1	
L_2		0.5	
H_E	15.6	16	16.4
HD	15.6	16	16.4
θ_2		12°	
θ_3		12°	
R		0.2	
R_1		0.2	
y			0.08

b Lead width of plated.
c Lead thickness of plated.
b1 Lead Width of basemetal.
c1 Lead thickness of basemetal.
* for reference

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
1.2	2002.11.14	H.NAKAYAMA	A.SATO	M.UCHIDA	

TITLE: TQFP15-100PIN [TQFP100-P-1414-0.5]

CAD FILE

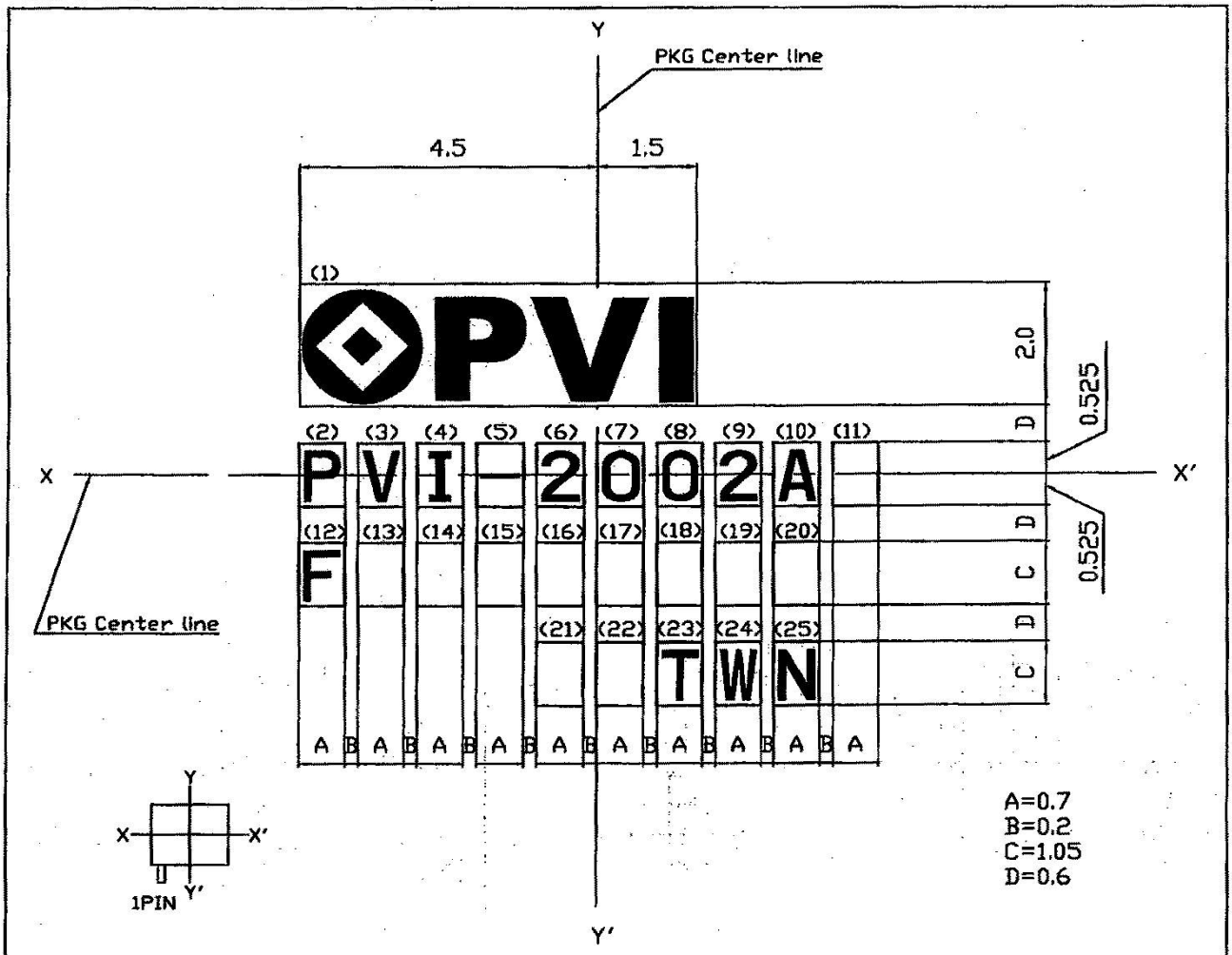
SEIKO EPSON CORP.

DWG No. 4900-0144

SCALE Free SHEET 1 of 1

2900-0002-01(Rev.1.1)

MARKING SPEC. 別紙 1



EXPLANATION OF MARK[:FIXED(固定)] S=10/1 1=1mm

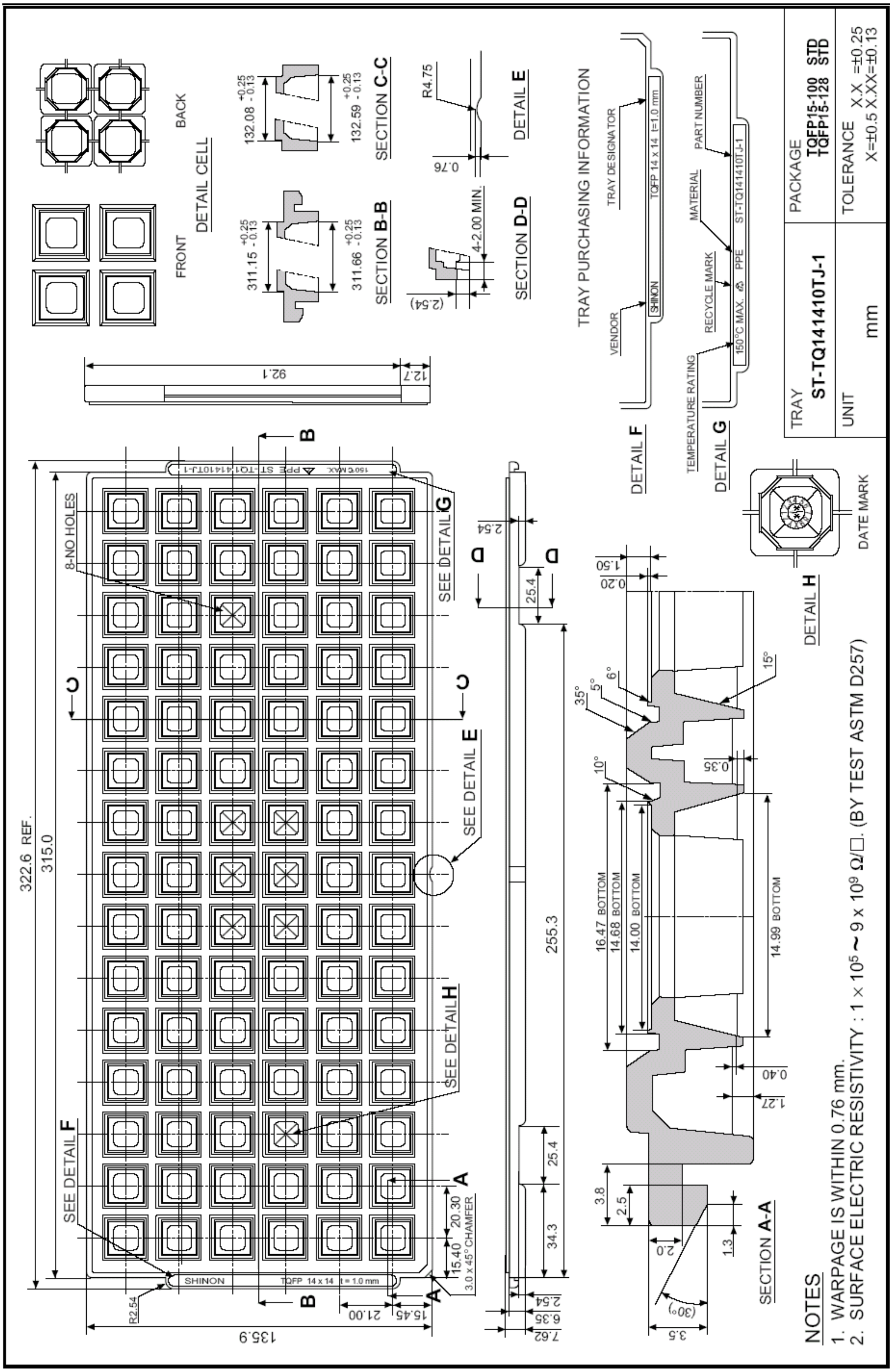
ITEM(項目)	No.	NOTE,(備考)
*CUSTOMER MARK(ユーザーマーク)	(1)	REFER TO LOGO TYPE FIXED(指定ロゴ使用)
*「TWN」	(21)~(25)	(21),(22)BLANK
*NAME OF GOODS(機種名)	(2)~(11)	(11)BLANK
CONTROL CODE(管理コード)	(12)~(20)	
*「F」	(12)	
YEAR OF MANUFACTURE(製造年)	(13)~(14)	LAST TWO NUMBER OF A.D.(西暦下2桁)
WEEK OF MANUFACTURE(製造週)	(15)~(16)	CALENDAR WEEK OF THE YEAR(1月1日を含む週01より追番)
W/F LOT No.	(17)~(20)	e.g. 0106 → 0106 IC生産管理部門より指定 1254 → 1254 される4桁のウェハロットNo. S352 → S352

QFP15 用

REV.	DATE	DESC.	APPD	CHEKD.	DRAW	CUSTOM	CONTENTS
			佐 03.6.4	本 03.6.-4	阿 03.6.-4		

NAME	PVI-2002A (S1L50552F32J000)
PACKAGE TYPE	TQFP15-100PIN
DEVICE CODE	
ASSEMBLY SPEC.	No.
TEMPLATE.	No. FTQ15M0002

SEIKO EPSON CORP. 0190-0117*付表-5-2*REV.5


DETAIL CELL
FRONT
BACK
132.08 +0.25 -0.13
132.59 +0.25 -0.13
SECTION C-C
311.15 +0.25 -0.13
311.66 +0.25 -0.13
SECTION B-B
R4.75
0.76
DETAIL E
4-2.00 MIN.
(2.54)
SECTION D-D
92.1
12.7
TRAY PURCHASING INFORMATION
VENDOR
TRAY DESIGNATOR
SHINON
TQFP 14 x 14 t=1.0 mm
DETAIL F
TEMPERATURE RATING
RECYCLE MARK
MATERIAL
PART NUMBER
150°C MAX.
PPE
ST-TQ141410TJ-1
DETAIL G
DATE MARK
DETAIL H
TRAY
ST-TQ141410TJ-1
UNIT
mm
PACKAGE
TQFP15-100 STD
TQFP15-128 STD
TOLERANCE X.X =±0.25
X=±0.5 X.XX=±0.13
8-NO HOLES
SEE DETAIL G
SEE DETAIL E
SEE DETAIL H
SEE DETAIL F
322.6 REF.
315.0
255.3
25.4
34.3
2.54
6.35
7.62
15.40
20.30
3.0 x 45° CHAMFER
R2.54
21.00
15.45
135.9
1.50
0.20
35°
5°
6°
10°
15°
0.35
16.47 BOTTOM
14.68 BOTTOM
14.00 BOTTOM
14.99 BOTTOM
0.40
1.27
3.8
2.5
2.0
1.3
(30°)
3.5
SECTION A-A
NOTES
1. WARPAGE IS WITHIN 0.76 mm.
2. SURFACE ELECTRIC RESISTIVITY : 1 × 10^5 ~ 9 × 10^9 Ω/□. (BY TEST ASTM D257)

10. Usage Precaution

10-1. Storage and handling before opening

Control the storage environment to prevent drastic temperature changes, which can lead to moisture condensation. Do not place any load on the package during storage.

10-2. Hygroscopic indicator monitoring

Because the appearance of normal silica gel do not change when absorbing moisture, a special blue gel manufactured by impregnating silica gel with cobalt chloride($CoCl_2$) is used as moisture absorption indicator. The molecular formula of this gel changes to $CoCl_2 \cdot 6H_2O$(pink) when it has absorbed moisture. Before mounting, you should check the silica gel condition.

10-3. Handling after opening

Do not bring any materials that can generate static electricity (plastic materials, chemical fibers, etc.) into the working area, and periodically check electrostatic conditions. Handle devices only with anti-statically treated materials or in conductive containers. Personnel should use wrist straps or other body grounding means.

10-4. Storage after opening

Due to the properties of the molding resin, plastic packages are prone to moisture absorption, also at room temperature if left for long periods of time. If the package is then inserted in the reflow oven while having absorbed moisture, cracks can develop in the resin, and joint between resin and lead frame can deteriorate. The standard storage periods for SMD packages shown below should therefore not be exceeded.

Table 10.1 Storage conditions after opening moisture proof packing

Storage rank	Storage condition after opening moisture proof packing	Guarantee period after opening moisture proof packing
SE 3	≤30℃/70% RH	Within 168 hours(1 week)

- Storage period before opening a moisture proof packing 12 months at less than ≤30℃/85% RH
- If reflow a package for 2 times, it should be done within storage periods for each package rank
- If the storage period is exceeded or it is undefined, perform baking again before mounting.

  Example : 125℃ for 24 hours (See section 10.5)

10-5. Baking

If the storage period is exceeded after opening, or if the opening data undefined, or if the hygroscopic indicator (blue gel) has turned pink, perform baking as indicated below.

Table 10.2 Baking conditions for surface mount devices

Package thickness \ Baking Temperature	125℃
t 〈 2 mm	5 hours
t ≥2 mm	24 hours

Note : Baking may be performed up to maximum of two times

10-6. Soldering conditions

When soldering surface mount devices using an overall soldering method such as reflow or vapor phase soldering, be sure to observe the storage conditions given in Table 10.1, This is important to prevent the possibility of crack and other damage, which increases if plastic package absorb moisture.

10-6-1 Infrared / air reflow

● Temperature profile

The temperature profile of the reflow oven (resin surface temperature) should be controlled as shown in Fig. 10.1

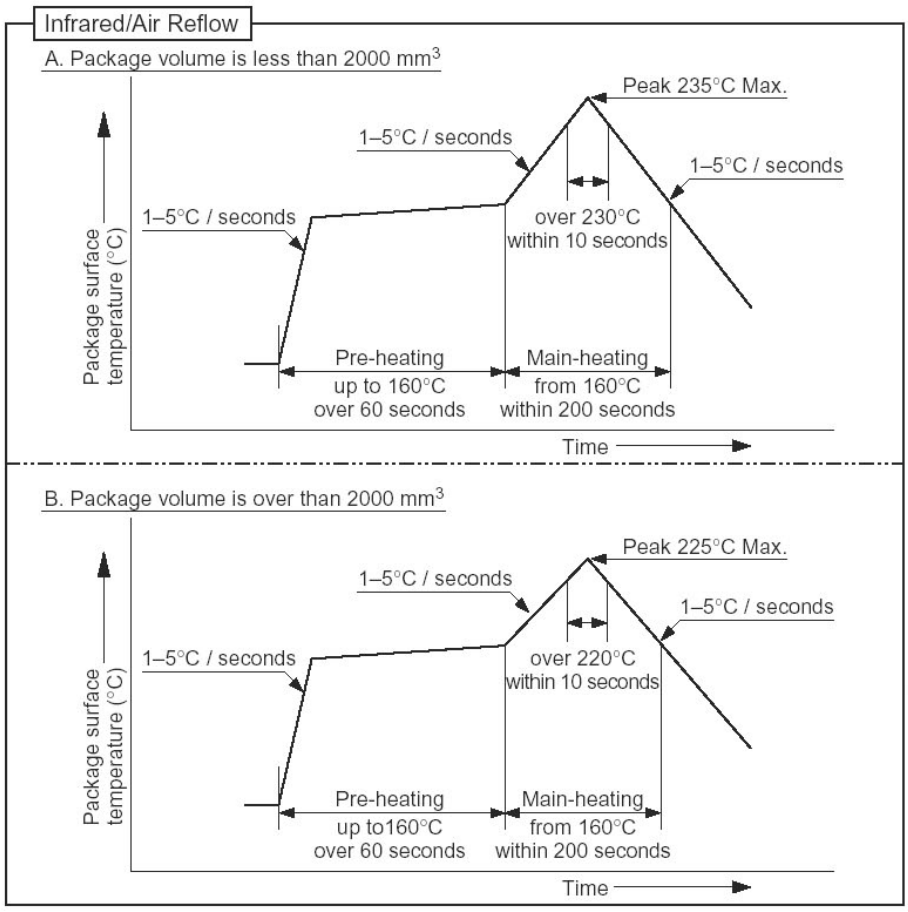


Fig. 10.1 Temperature profile for standard SMD package

● Maximum temperature

The maximum resin surface temperature should be 235 ℃, for a duration of 10 seconds or less. If possible, lower temperatures and shorter times are preferable.

10-6-2 Vapor phase reflow

● Temperature profile

The temperature profile of the vapor phase reflow oven (resin surface temperature) should be controlled as shown in Fig. 10.2

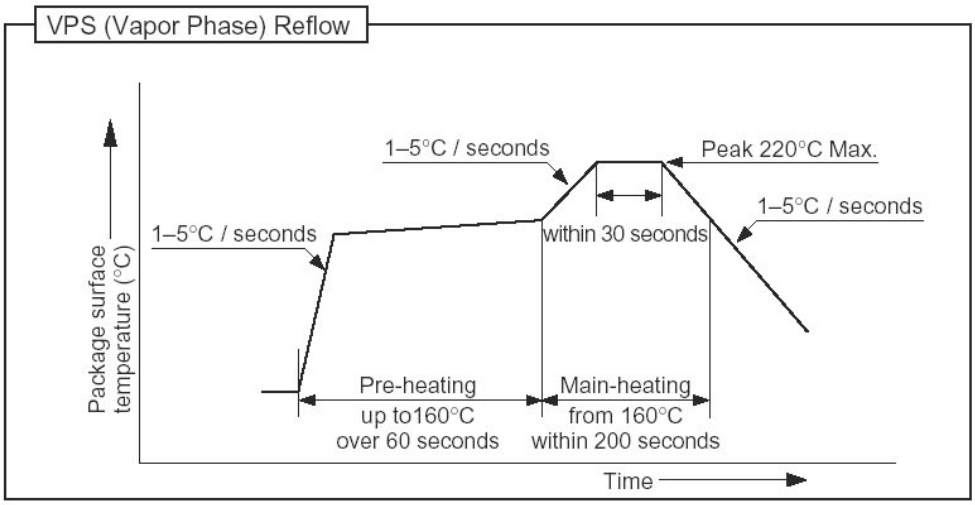


Fig. 10.2 Temperature profile for standard SMD package

● Temperature rise ratio

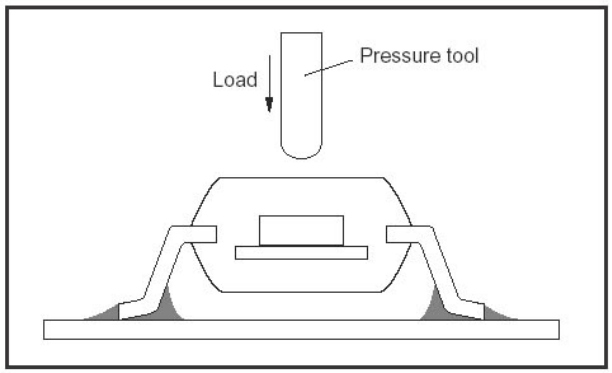
The maximum rise should be kept within 1- 5 ℃/minute, and the curve should be as shallow as possible.

10-6-3 Solder dipping (wave soldering etc)

Because solder dipping cause a drastic change in package temperature which can damage the device, Seiko Epson normally does not approve solder dipping methods for SMD. However, certain SOP with good heat resistance may be mounted using solder dipping.

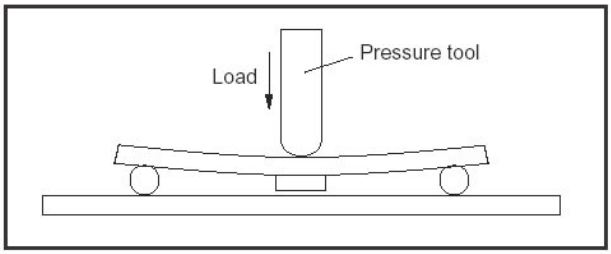
10-7 Mounting Precautions

Mechanical stress during mounting should be minimized (EIAJ-ED-4702)



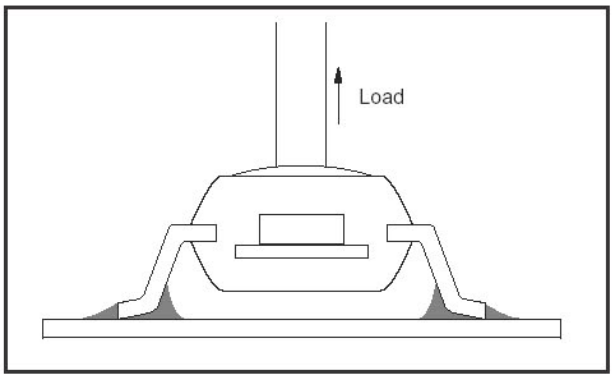
① Package load
The force exerted on the package surface during mounting should not exceed 1 kgf (10 N).

Fig. 10.3 Package Strength



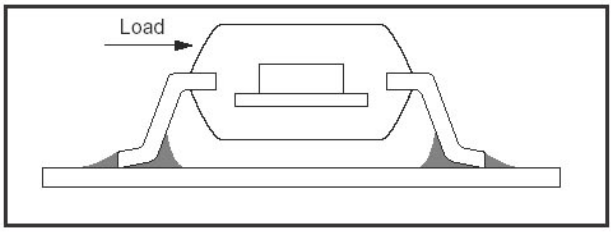
② PCB bending stress
For reasons of solder junction strength, PCB deflection after mounting should not exceed 2 mm.

Fig. 10.4 PCB Bending Strength



③ Pull load
Pull stress (sudden force exerted on the package in vertical up direction) after mounting should not exceed 0.5 kgf (5 N).

Fig. 10.5 Pull Strength



④ Sticking stress
Sticking stress (sudden force exerted on the package in sideways direction) after mounting should not exceed 0.5 kgf (5 N).

Fig. 10.6 Sticking Strength

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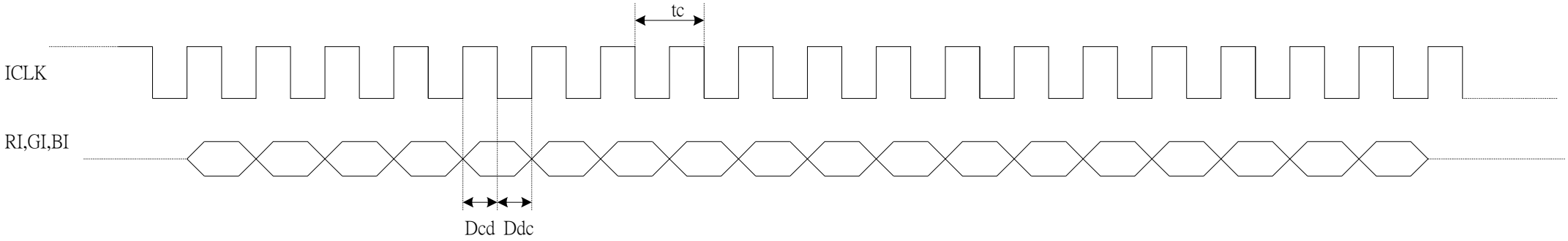
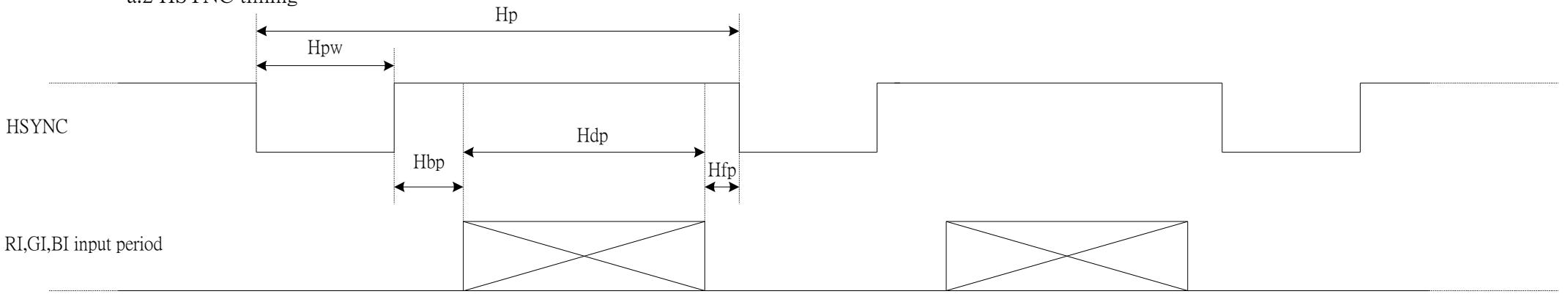
A. The timing diagram

a. Input signal range

a.1 ICLK,RI,GI,BI relationship

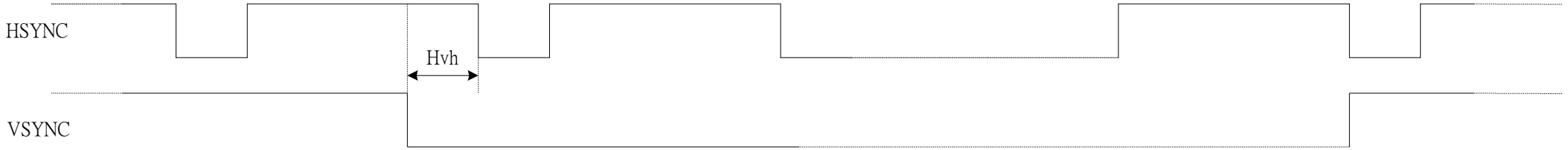


a.2 HSYNC timing

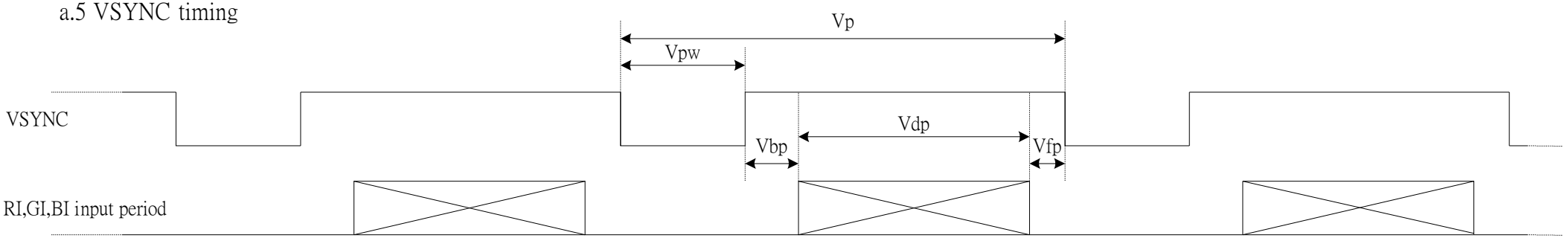


a.3 ICLK,HSYNC relationship

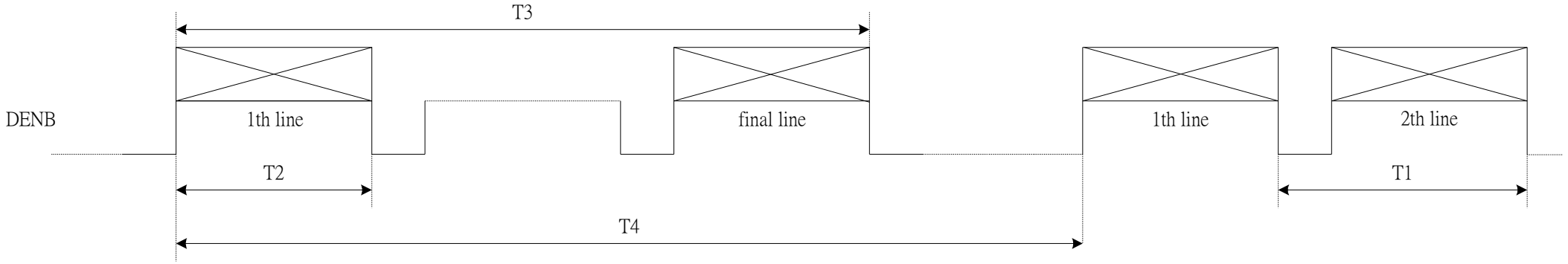
a.4 HSYNC,VSYNC relationship



a.5 VSYNC timing

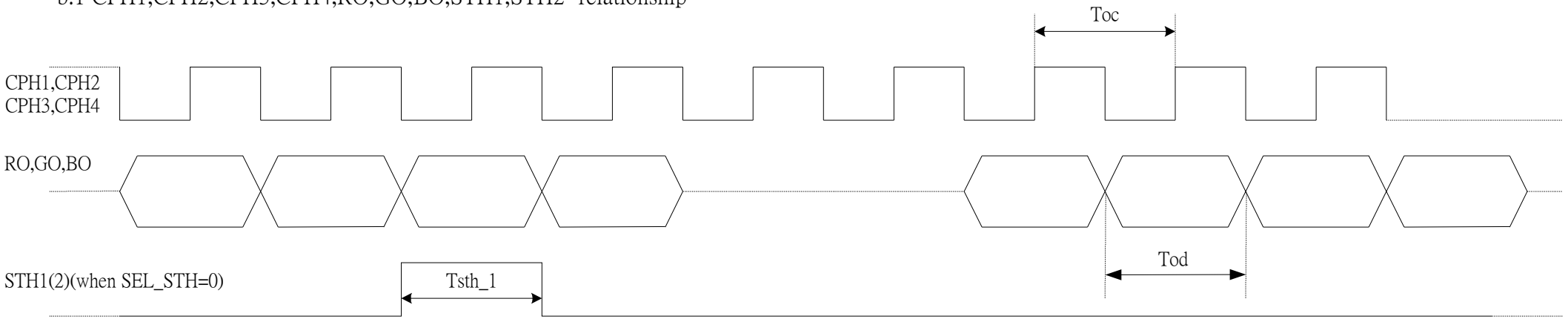


a.6 DENB timing

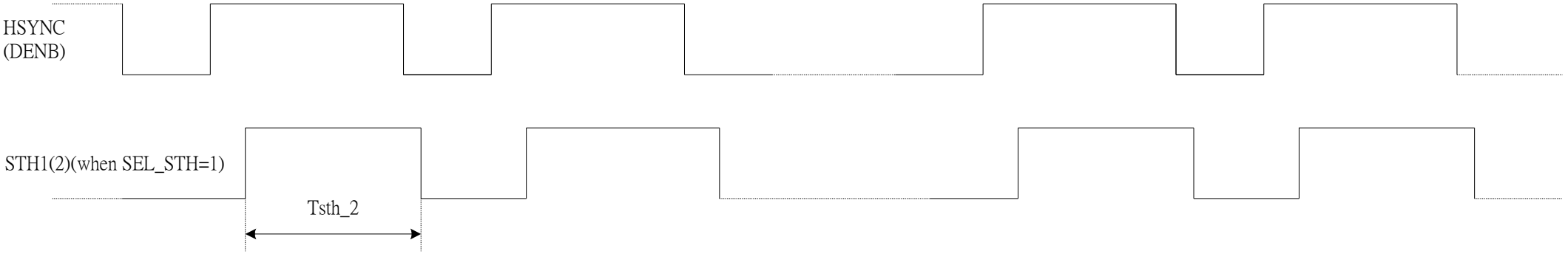


b. Output signal timing(when input signal equal typ. value)

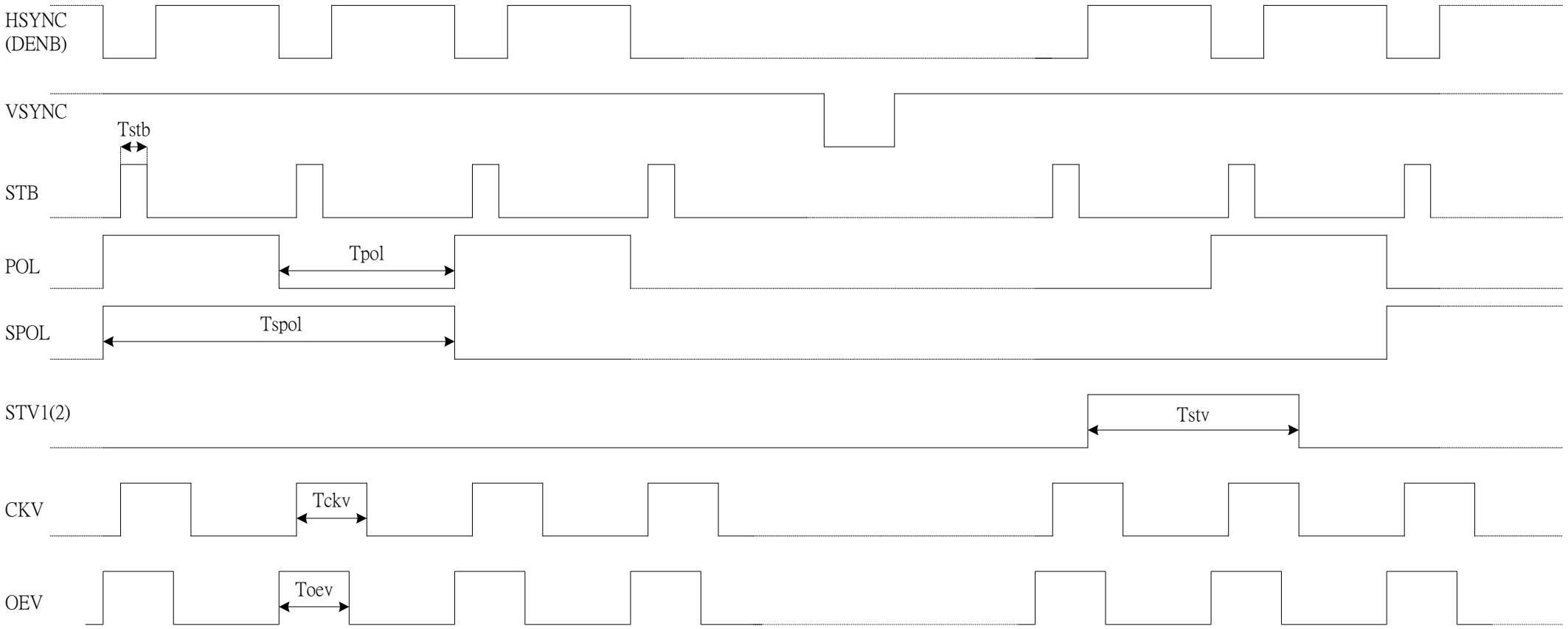
b.1 CPH1,CPH2,CPH3,CPH4,RO,GO,BO,STH1,STH2 relationship



b.2 HSYNC,DENB,STH1,STH2 relationship

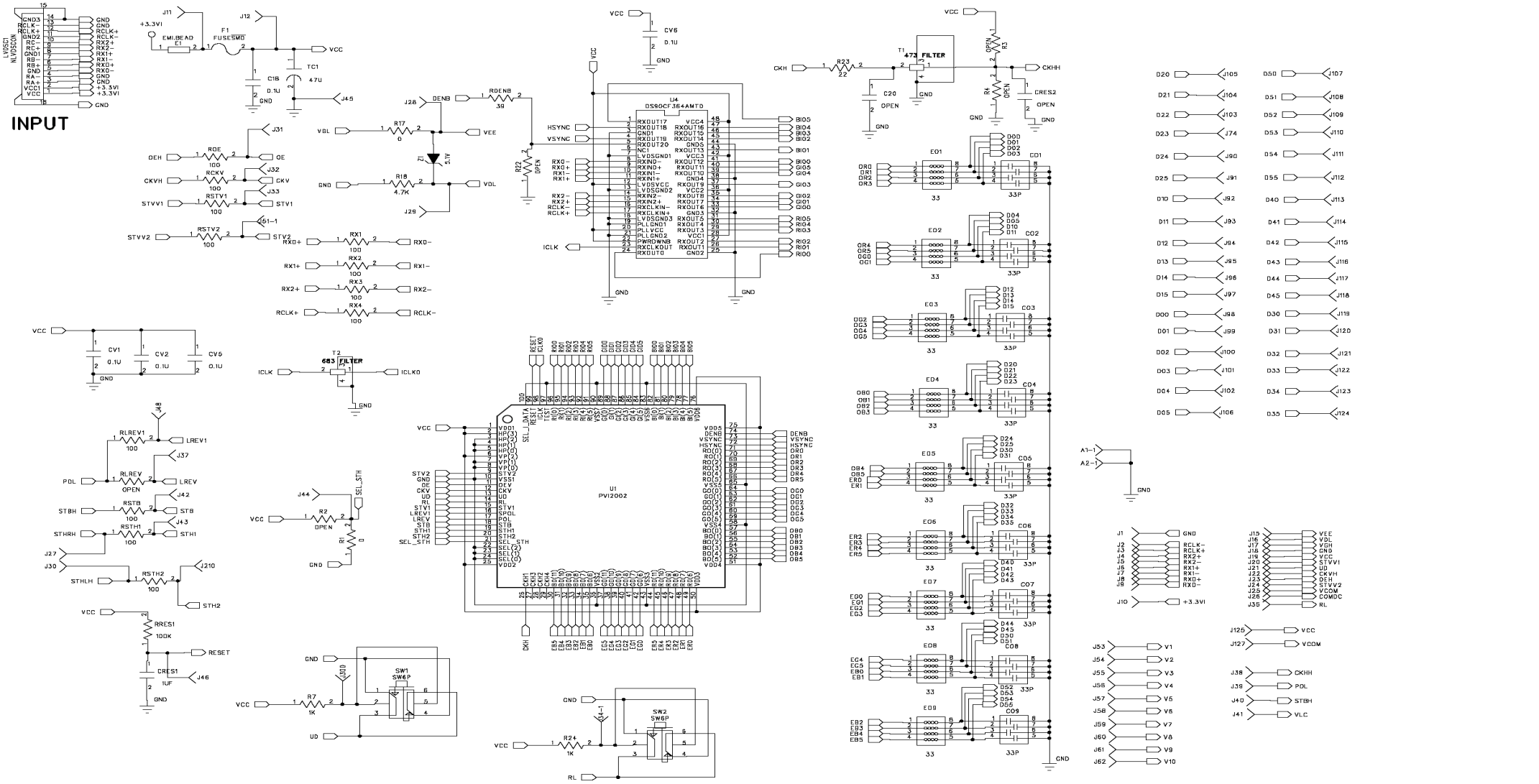


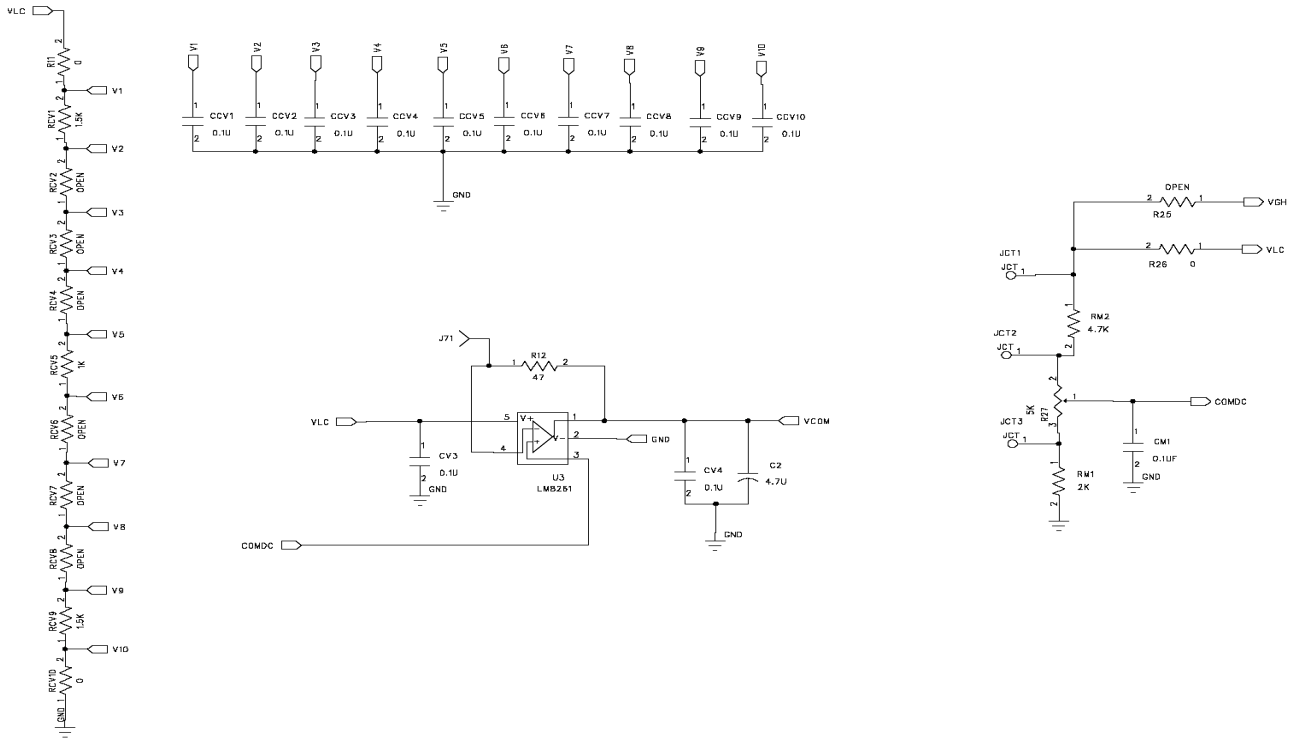
b.3 HSYNC,VSYNC,DENB,STB,POL,SPOL,CKV,OEV,STV1,STV2 relationship



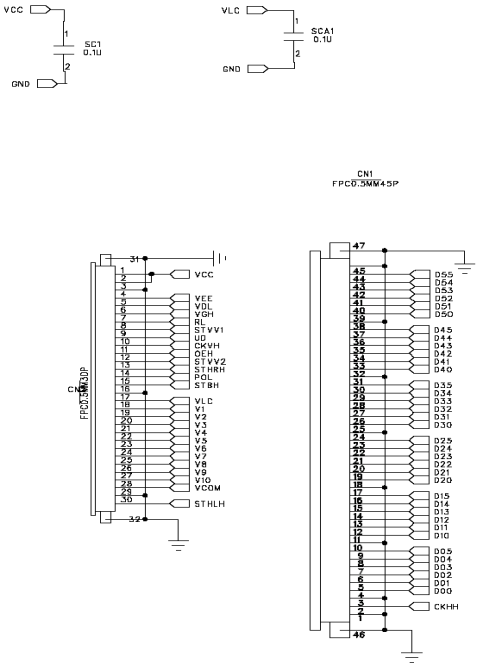
B. Application circuit

a.1 10.4 吋 SVGA reference circuit in next four continuous pages.



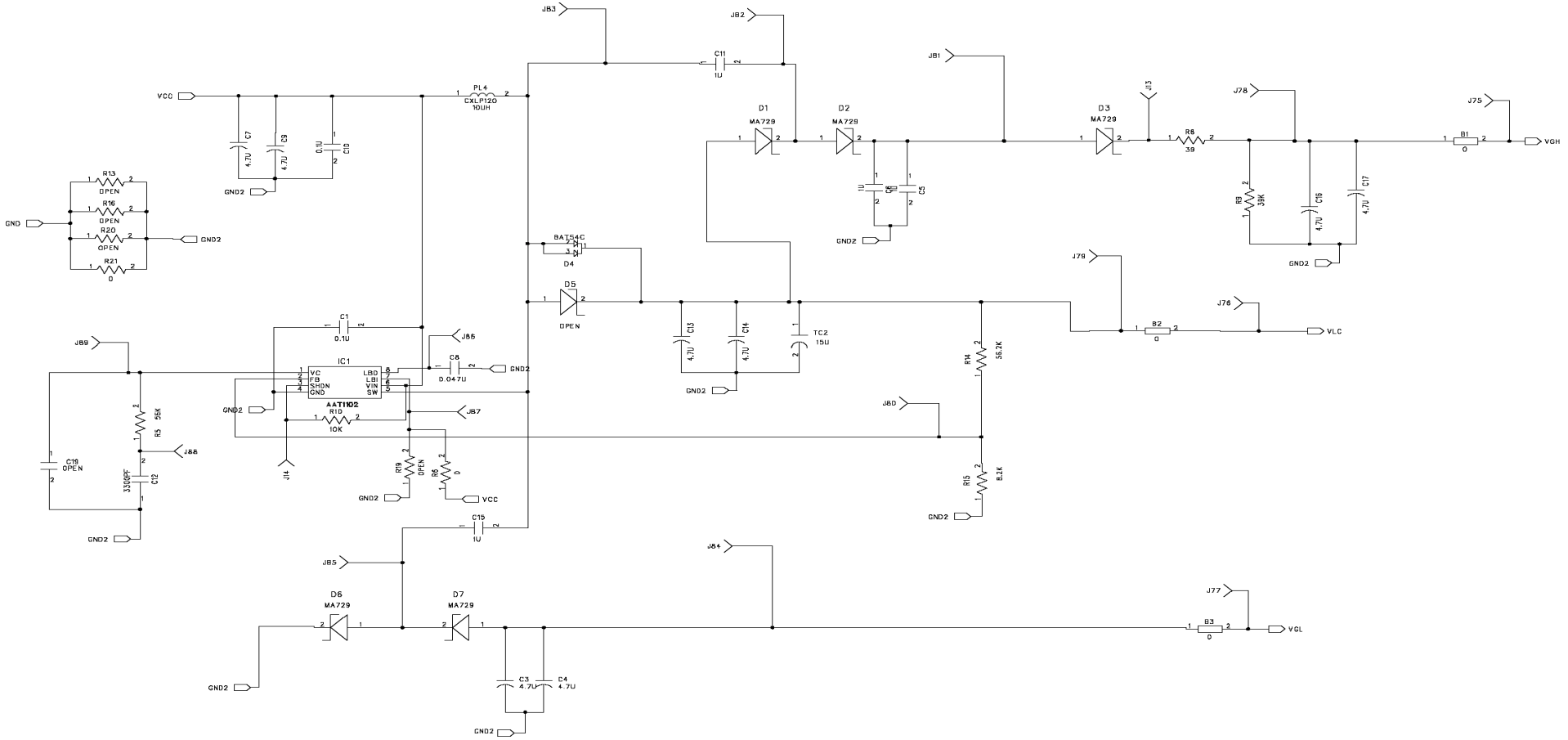


TITLE: Gamma & VCOM circuit		
Document Number: 10.4" SVGA(PVI-2002A)		Rev. 1.0
Date: Dec/17/2004	Sheet 2 of 4	



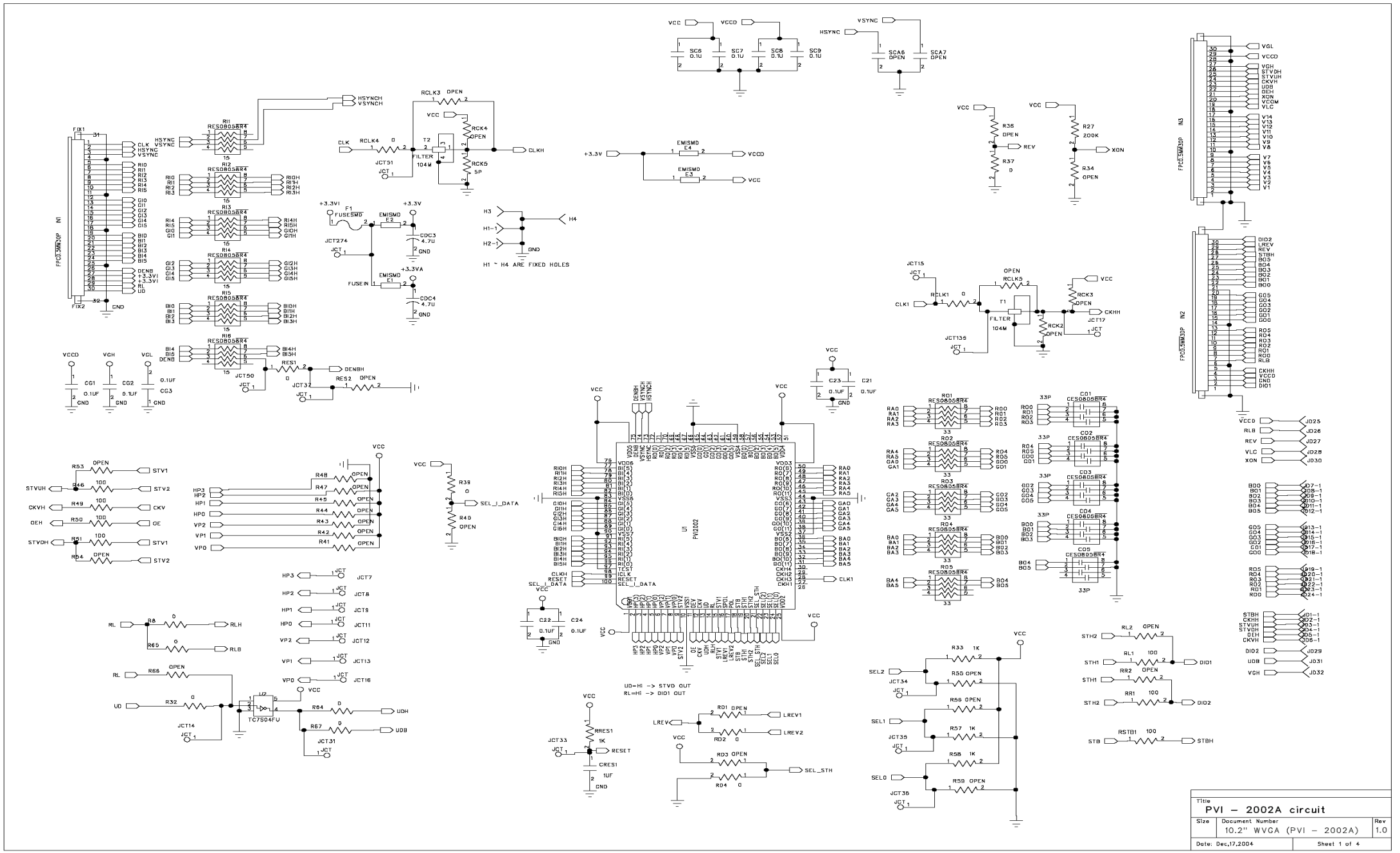
Output to PANEL

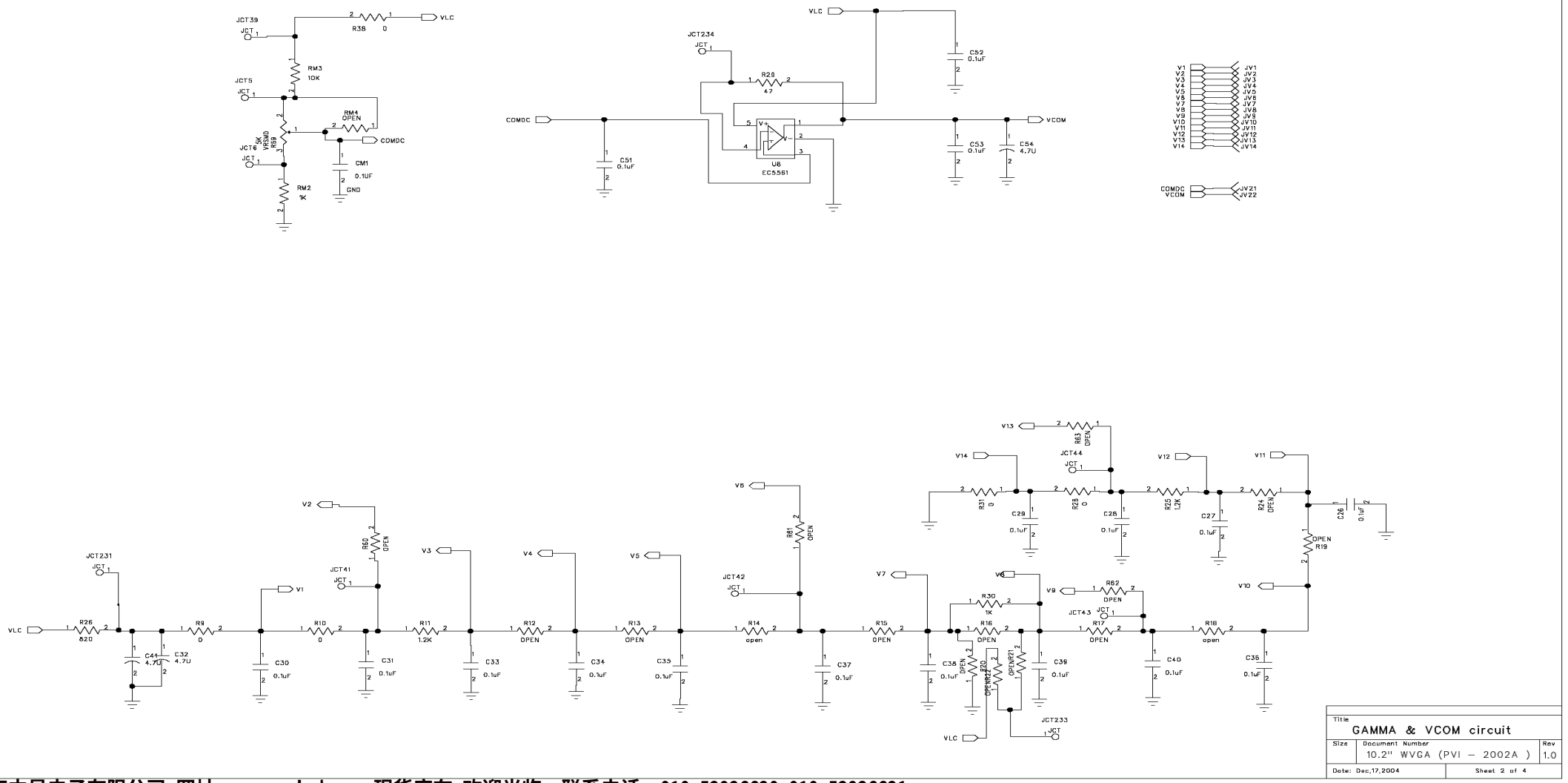
TITLE: FPC connector to PANEL		
Document Number: 10.4" SVGA(PVI-2002A)		Rev. 1.0
Date: Dec/17/2004	Sheet 3 of 4	

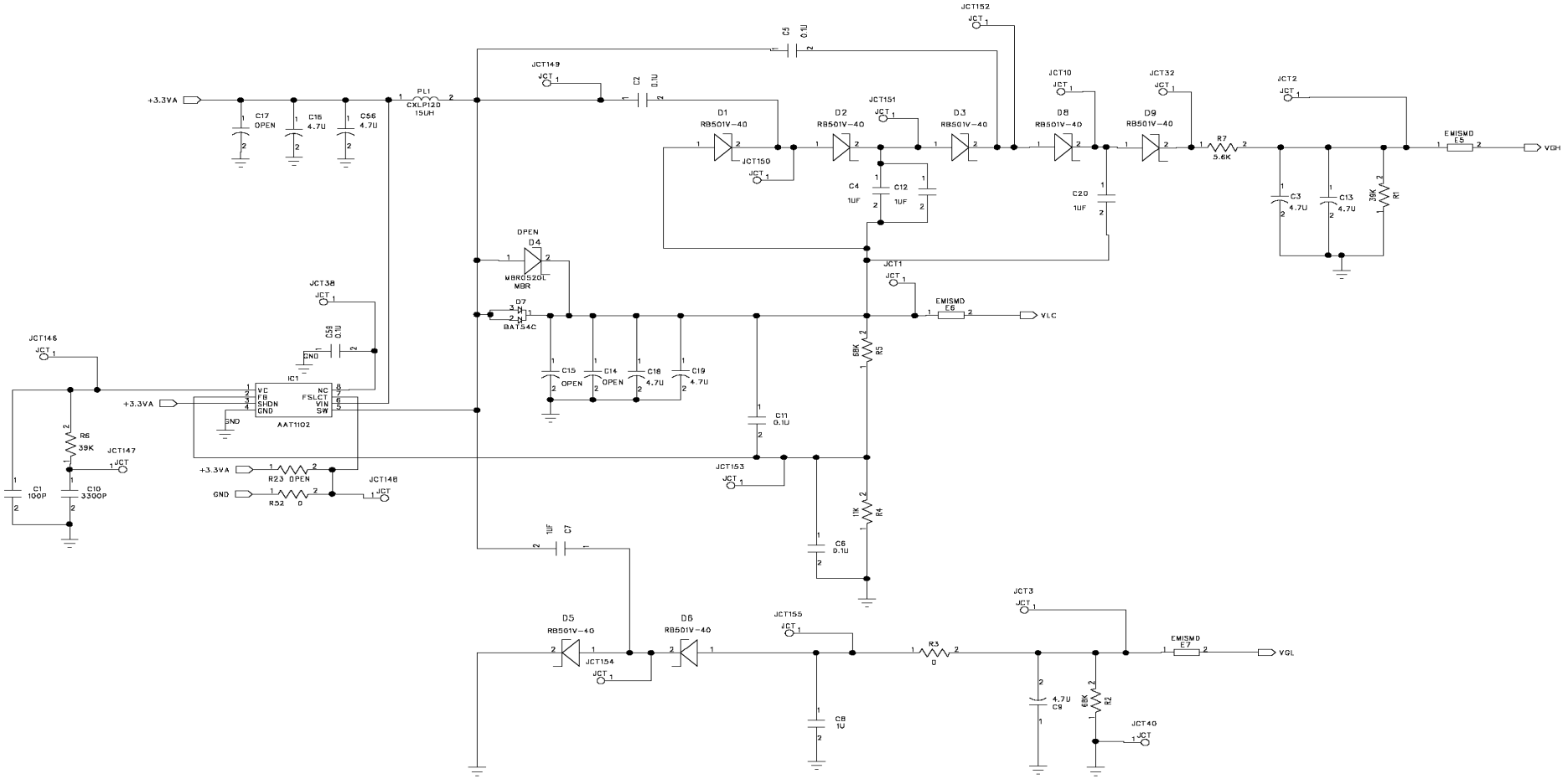


TITLE: DC/DC Converter		
Document Number: 10.4" SVGA(PVI-2002A)		Rev. 1.0
Date: Dec/17/2004	Sheet 4 of 4	

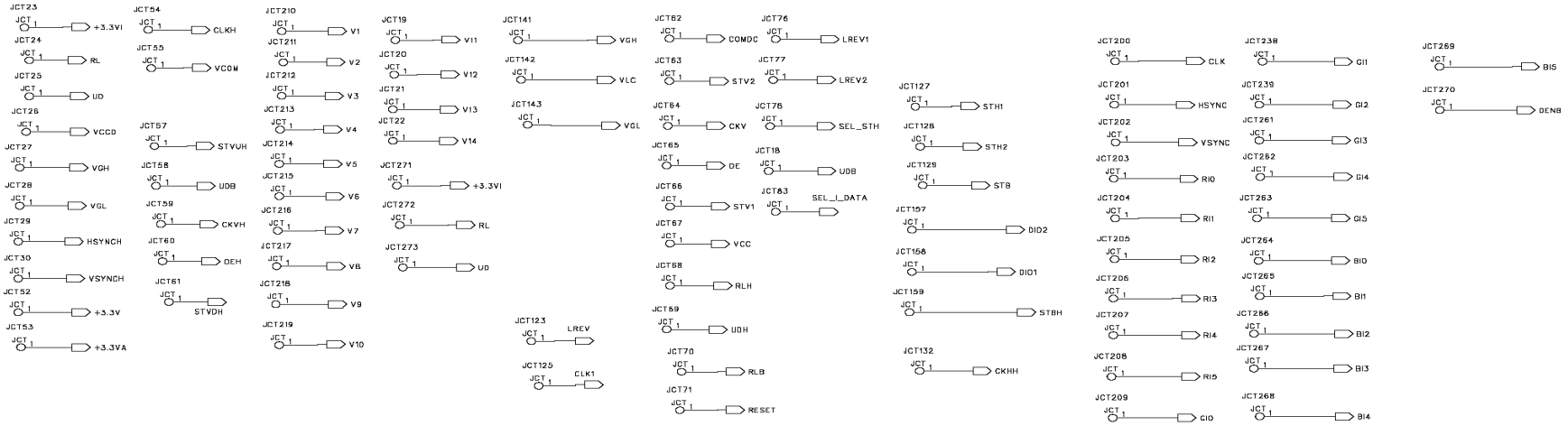
a.2 10.2 吋 WVGA reference circuit in next four continuous pages.


Title
PVI – 2002A circuit
Size
Document Number
10.2" WVGA (PVI – 2002A)
Rev
1.0
Date: Dec,17,2004
Sheet 1 of 4



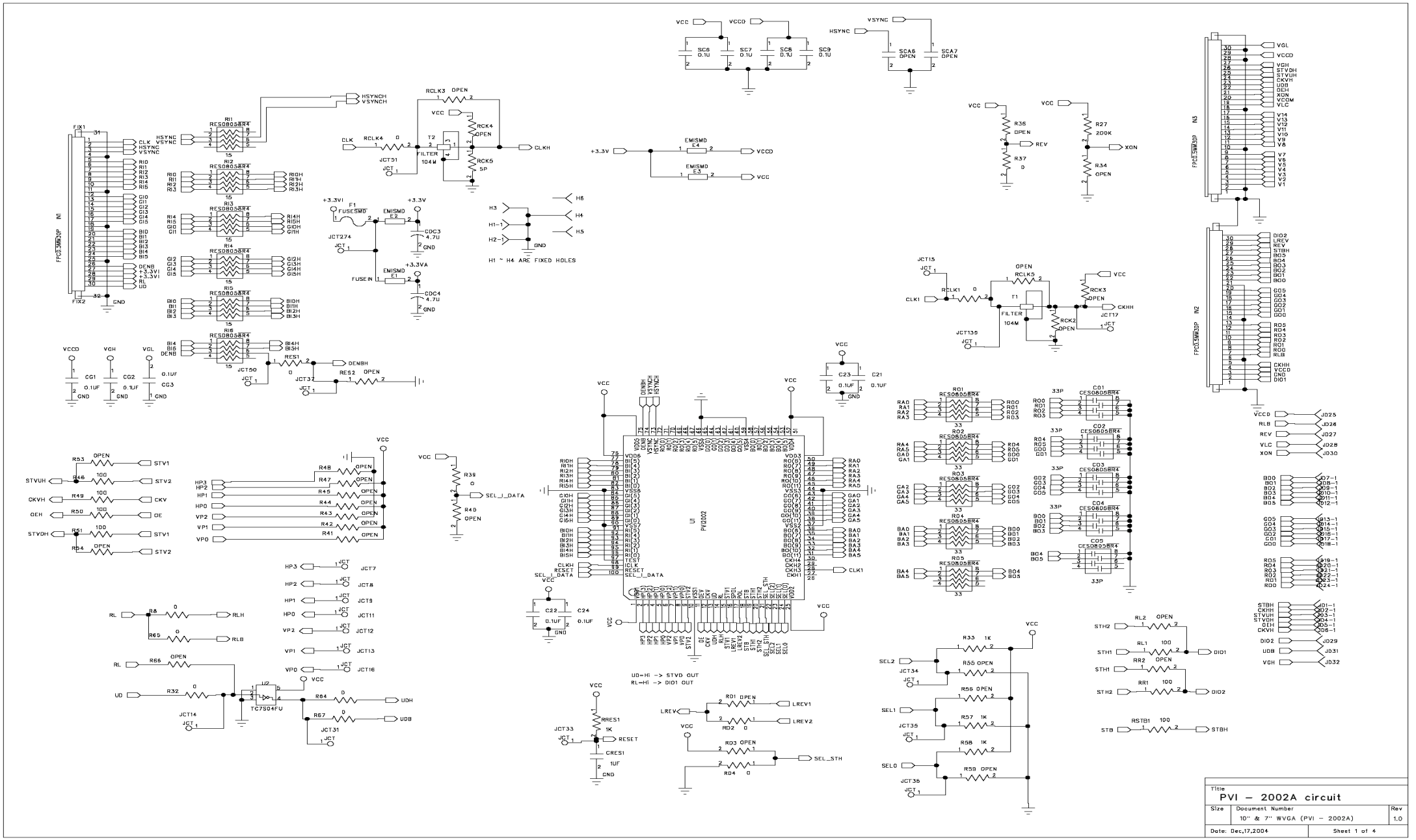


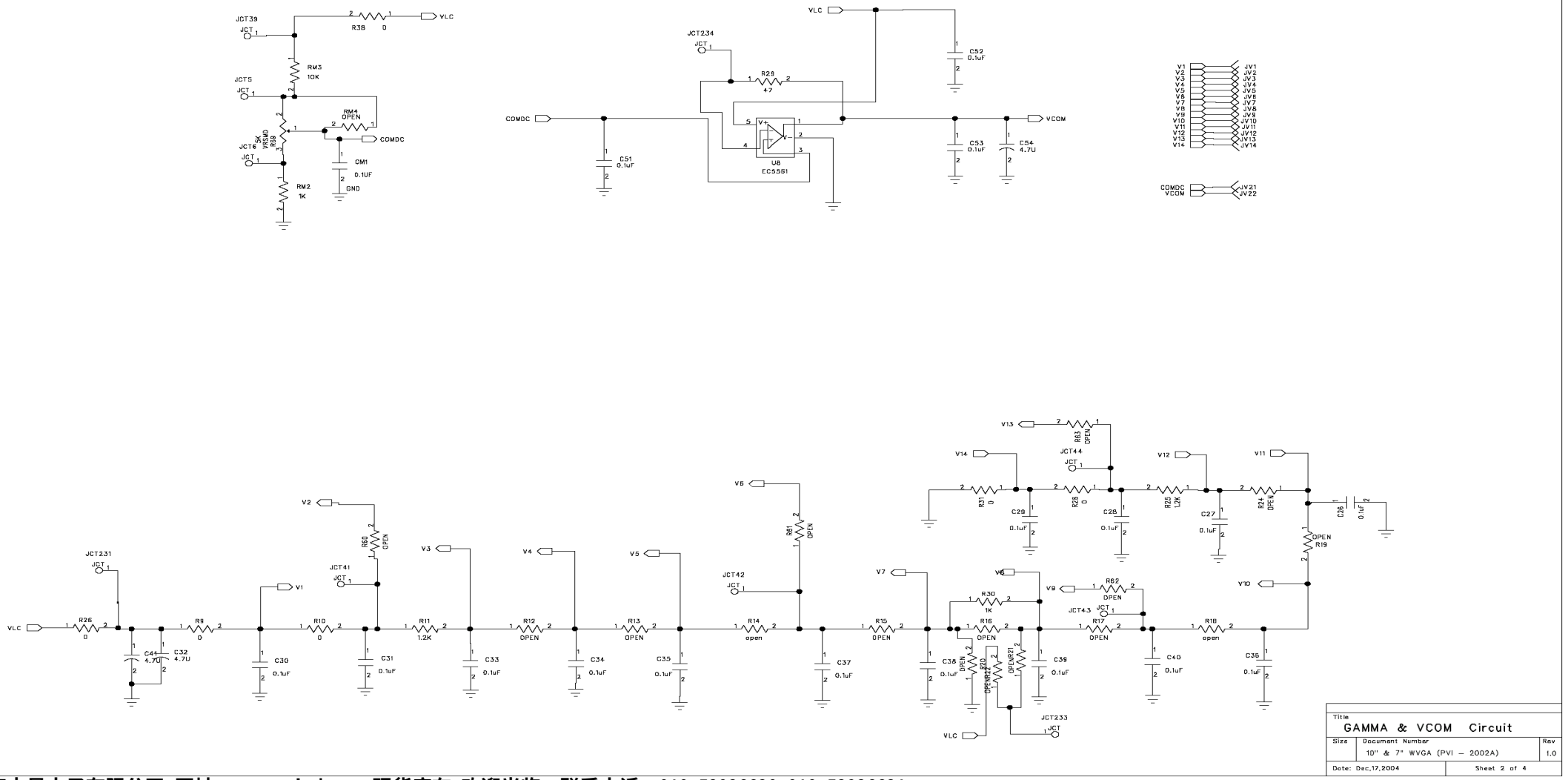
Title: POWER DC-DC circuit		
Size	Document Number: 10.2" WVGA (PVI - 2002A)	Rev: 1.0
Date: Dec,17,2004	Sheet 3 of 4	

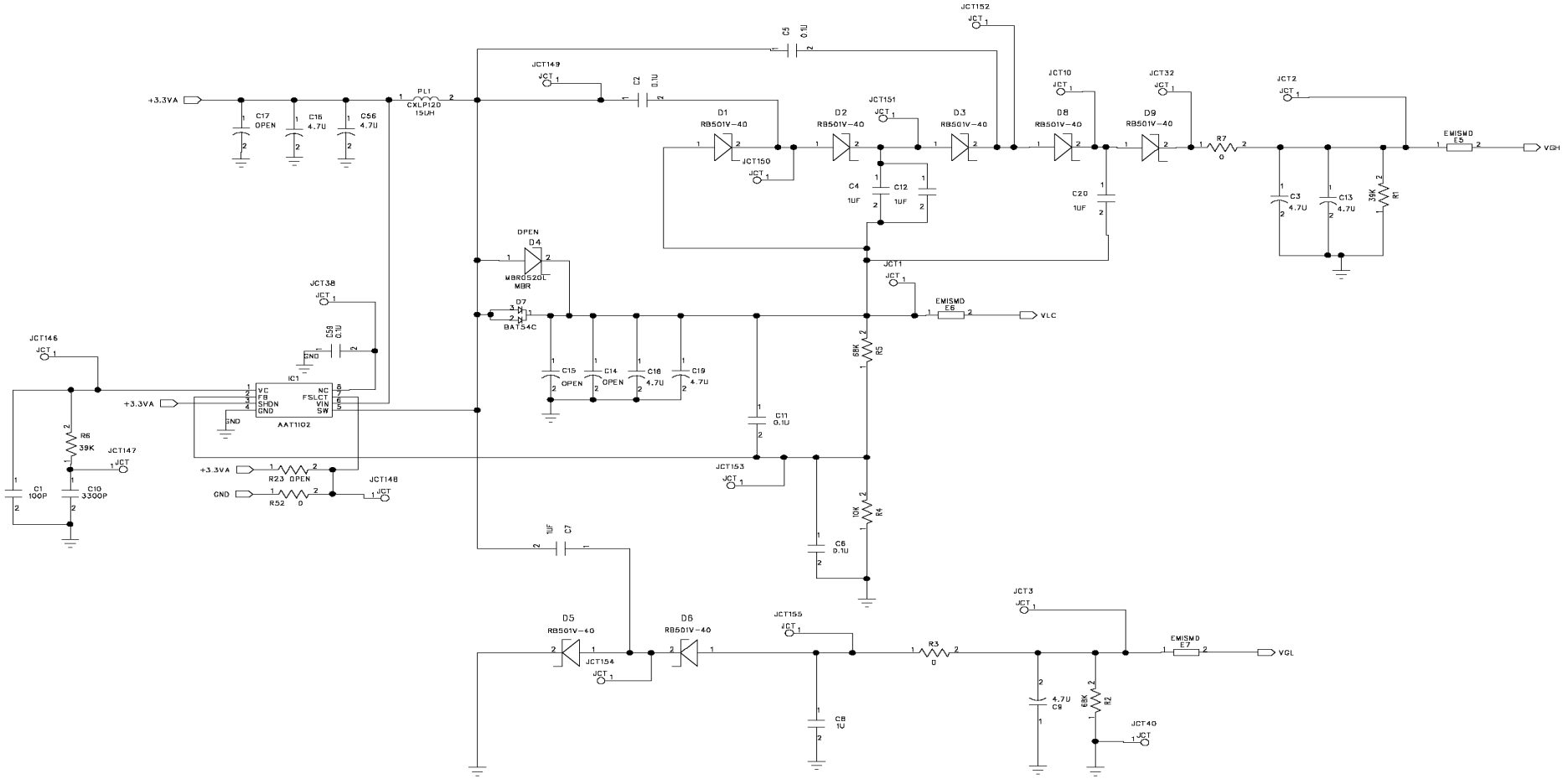


Title: ICT Test Point		
Size	Document Number: 10.2" WVGA (PVI – 2002A)	Rev: 1.0
Date: Dec,17,2004	Sheet 4 of 4	

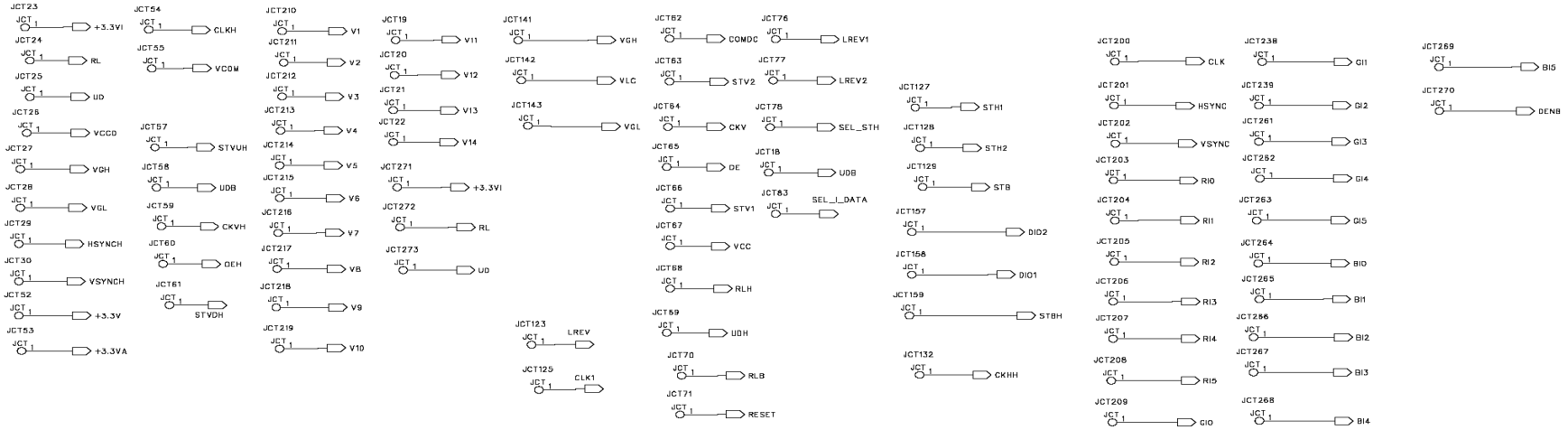
a.3 10吋 & 7吋 WVGA reference circuit in next four continuous pages.


PVI-2002
Title
PVI – 2002A circuit
Size
Document Number
10" & 7" WVGA (PVI – 2002A)
Rev
1.0
Date: Dec,17,2004
Sheet 1 of 4
H1 ~ H4 ARE FIXED HOLES
UD=Hi -> STVD OUT
RL=Hi -> DIO1 OUT



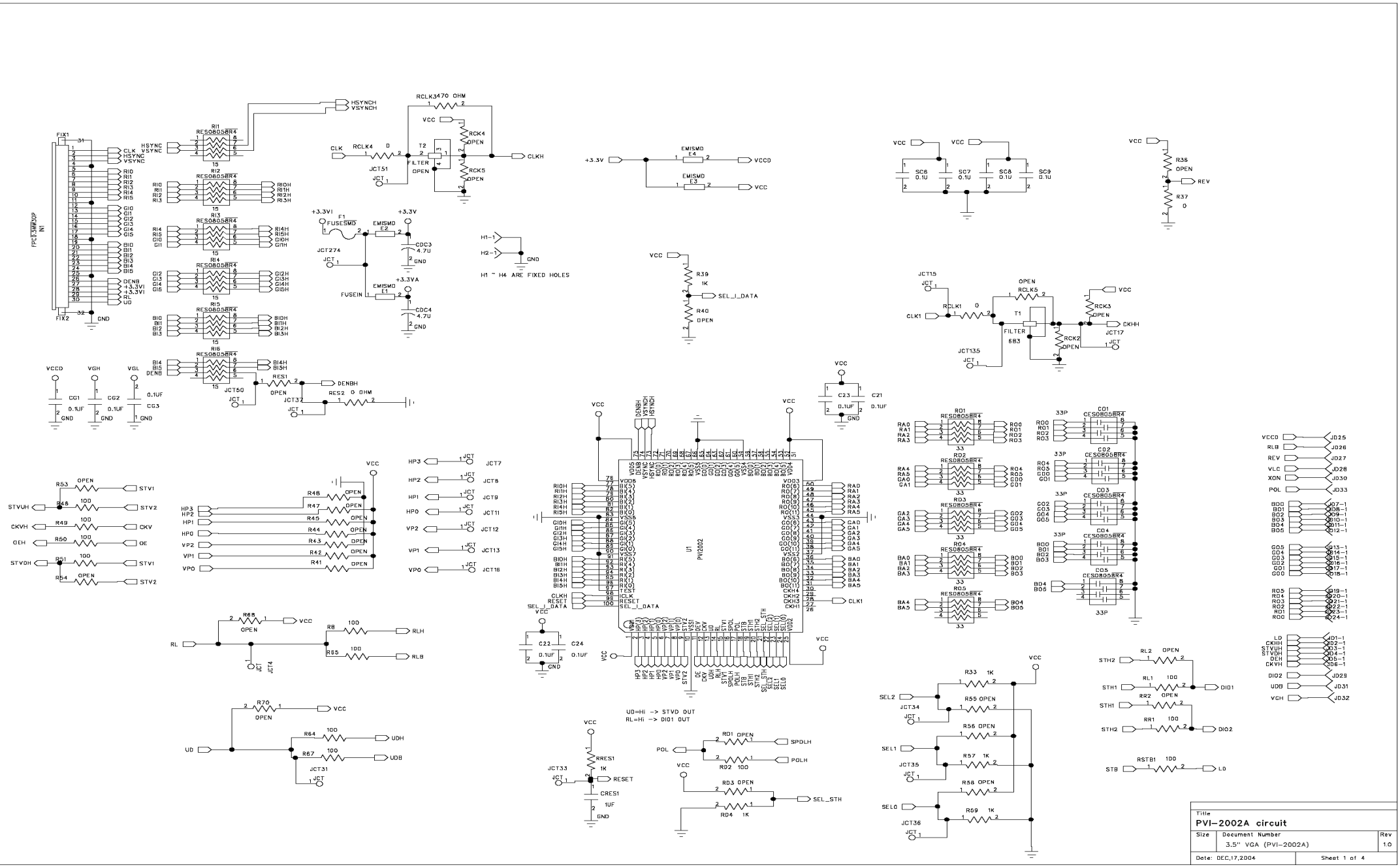


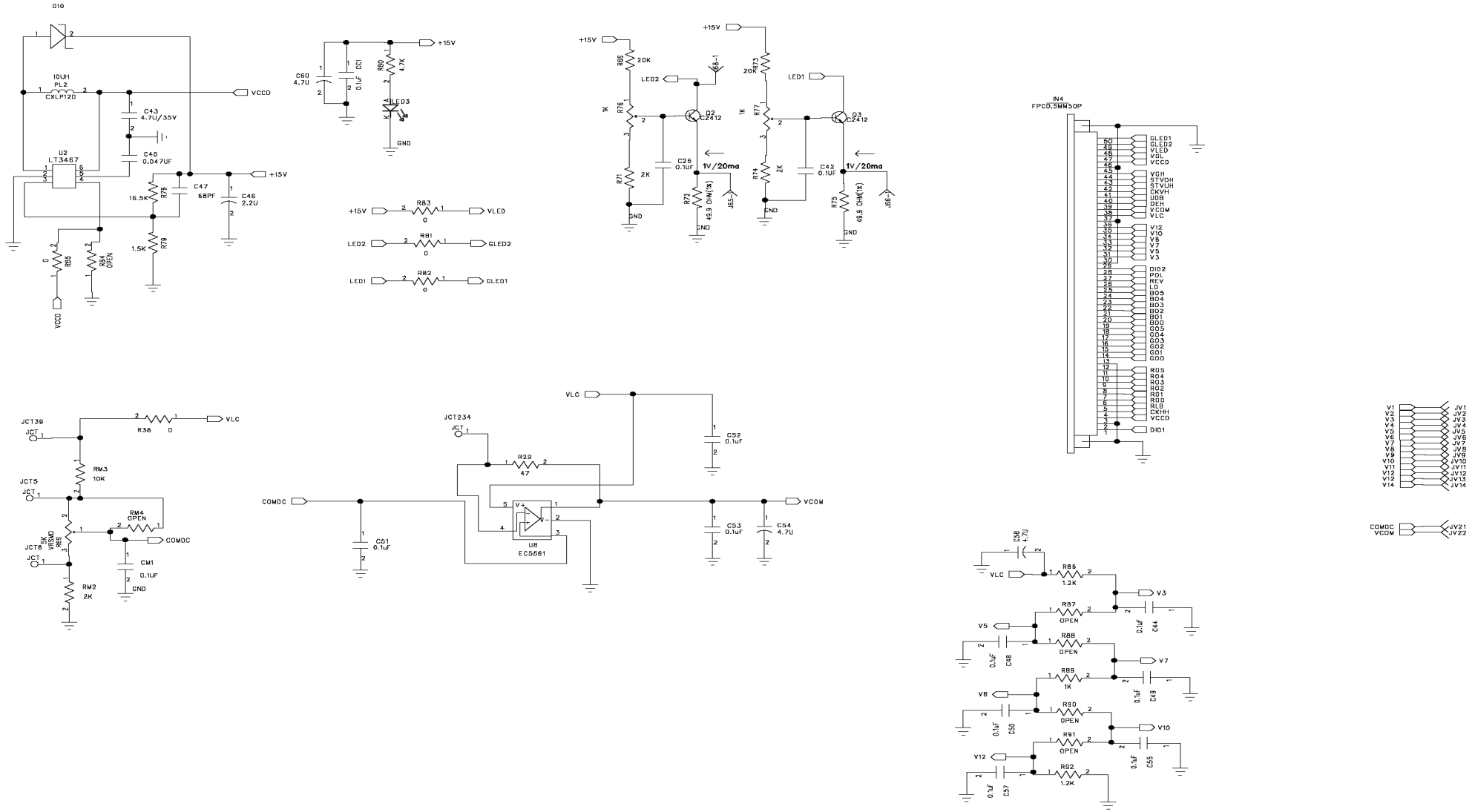
Title: POWER DC-DC circuit		
Size	Document Number: 7" & 10" WVGA (PVI - 2002A)	Rev: 1.0
Date: Dec,17,2004	Sheet 3 of 4	



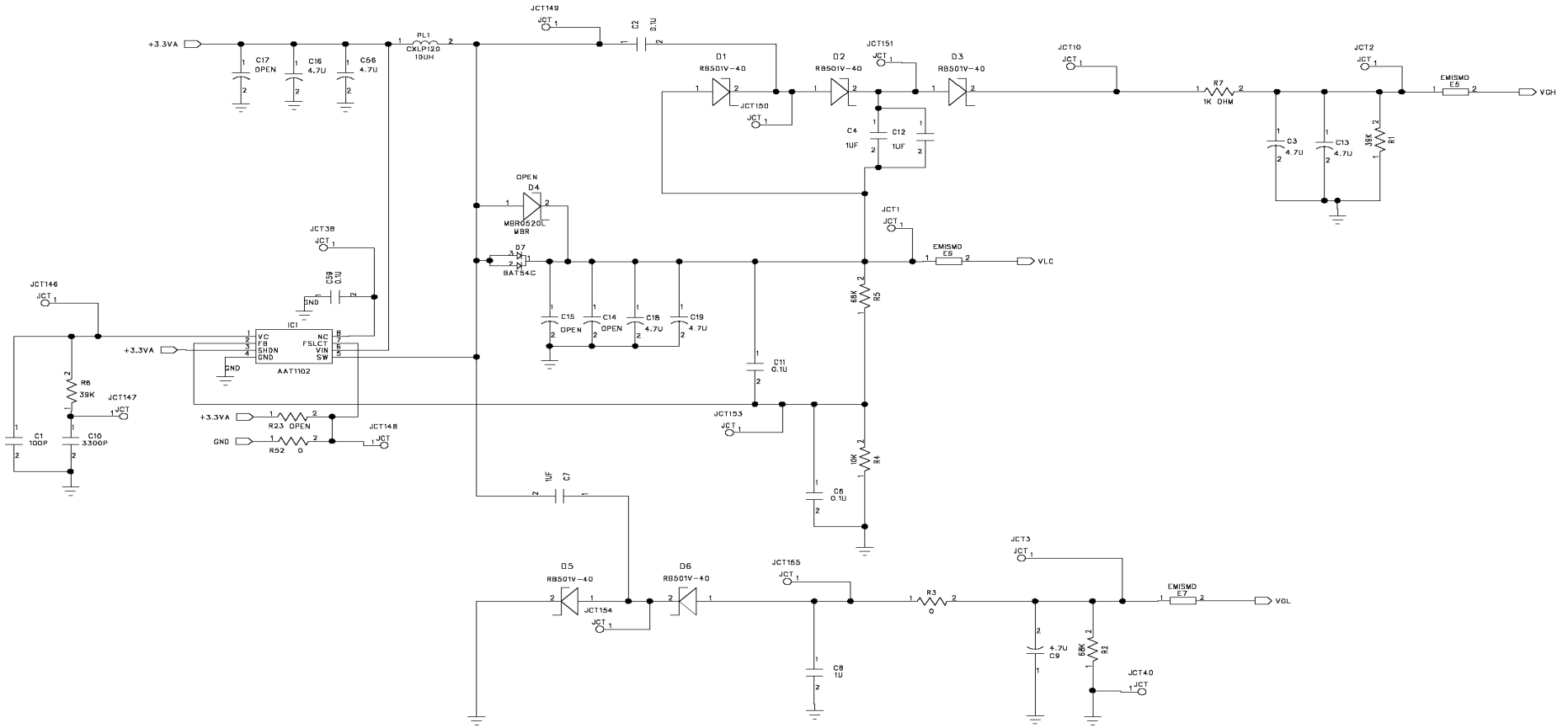
Title: ICT Test Point		
Size	Document Number: 7" & 10" WVGA (PVI – 2002A)	Rev: 1.0
Date: Dec,17,2004	Sheet 4 of 4	

a.4 3.5 吋 VGA reference circuit in next four continuous pages.

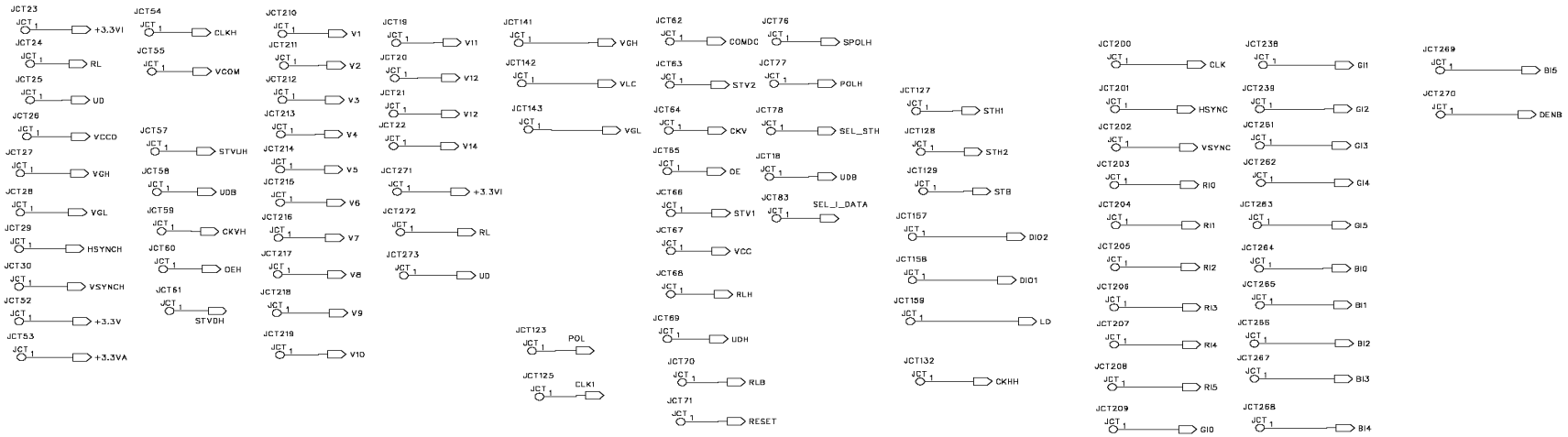

HSYNCH
VSYNCH
RCLK3 470 OHM
RCK4 OPEN
RCK5 OPEN
CLKH
EMISMD E4
EMISMD E3
VCCD
SC6 0.1U
SC7 0.1U
SC8 0.1U
SC9 0.1U
R35 OPEN
REV
R37 0
FIX1
FIX2
GND
RI1 RESO805BR4
RI2 RESO805BR4
RI3 RESO805BR4
RI4 RESO805BR4
RI5 RESO805BR4
RI6 RESO805BR4
+3.3V1
FUSESMD F1
EMISMD E2
EMISMD E1
CDC3 4.7U
CDC4 4.7U
+3.3VA
FUSEIN
H1~H4 ARE FIXED HOLES
R39 1K
SEL_I_DATA
R40 OPEN
JCT15
RCLK1 0
RCLK5 OPEN
RCK3 OPEN
RCK2 OPEN
FILTER
6B3
CKHH
JCT135
JCT17
VCCD
VGH
VGL
CG1 0.1UF
CG2 0.1UF
CG3 0.1UF
JCT50
RES1 OPEN
RES2 0 OHM
DENBH
JCT32
C23
C21 0.1UF
RD1 RESO805BR4
RD2 RESO805BR4
RD3 RESO805BR4
RD4 RESO805BR4
RD5 RESO805BR4
CD1 CESO805BR4
CD2 CESO805BR4
CD3 CESO805BR4
CD4 CESO805BR4
CD5 CESO805BR4
33P
33
R53 OPEN
R48 100
R49 100
R50 100
R51 100
R54 OPEN
STV1
STV2
CKV
OE
STVDH
STVUH
CKVH
OEH
HP3
HP2
HP1
HP0
VP2
VP1
VP0
JCT7
JCT8
JCT9
JCT11
JCT12
JCT13
JCT16
R47 OPEN
R45 OPEN
R44 OPEN
R43 OPEN
R42 OPEN
R41 OPEN
U1
PVI2002
C22 0.1UF
C24 0.1UF
R65 OPEN
R8 100
R85 100
RLH
RLB
RL
JCT4
R70 OPEN
R64 100
R67 100
UDH
UDB
UD
JCT31
UD=Hi -> STVD OUT
RL=Hi -> DIO1 OUT
RRES1 1K
CRES1 1UF
RESET
JCT33
RD1 OPEN
RD2 100
SPDLH
POLH
POL
RD3 OPEN
RD4 1K
SEL_STH
R33 1K
R55 OPEN
R56 OPEN
R57 1K
R58 OPEN
R59 1K
SEL2
SEL1
SEL0
JCT34
JCT35
JCT36
RL2 OPEN
RL1 100
RR2 OPEN
RR1 100
RSTB1 100
STH2
STH1
DIO1
DIO2
STB
LD
VCCD
RLB
REV
VLC
XON
POL
BD0
BD1
BD2
BD3
BD4
BD5
GD5
GD4
GD3
GD2
GD1
GD0
RD5
RD4
RD3
RD2
RD1
RD0
LD
CKHH
STVUH
STVDH
DEH
CKVH
DIO2
UDB
VGH
JD25
JD26
JD27
JD28
JD30
JD33
JD7-1
JD8-1
JD9-1
JD10-1
JD11-1
JD12-1
JD13-1
JD14-1
JD15-1
JD16-1
JD17-1
JD18-1
JD19-1
JD20-1
JD21-1
JD22-1
JD23-1
JD24-1
JD1-1
JD2-1
JD3-1
JD4-1
JD5-1
JD6-1
JD29
JD31
JD32
Title
PVI-2002A circuit
Size
Document Number
3.5" VGA (PVI-2002A)
Rev
1.0
Date: DEC,17,2004
Sheet 1 of 4



Title: Gamma RES. & LED Power circuit		
Size	Document Number: 3.5" VGA (PVI2002A)	Rev: 1.0
Date: DEC,17,2004	Sheet 2 of 4	



Title: DC–DC POWER circuit		
Size	Document Number: 3.5" VGA (PVI–2002A)	Rev: 1.0
Date: Dec,17,2004	Sheet 3 of 4	



Title: ICT TEST POINT		
Size	Document Number: 3.5'' VGA (PVI-2002A)	Rev: 1.0
Date: Dec,8,2004	Sheet 4 of 4	

Revision History

Rev.	Issued Date	Revised Contents
1.0	Oct/17/2003	New
1.1	Nov/18/2003	Modify 1. Add 10”(WVGA) reference circuit
1.2	Dec/17/2004	Modify 1. Add 10.4”(SVGA)、10.2”(WVGA)、7”(WVGA)、3.5”(VGA) reference circuit 2. Delete 6.4”(VGA) reference circuit 3. Add Revision History